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SiGeO layer formation mechanism at the SiGe/oxide interfaces during Ge condensation

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The letter presents the fabrication processes to realize high Ge content SiGe on insulator using Ge condensation technique with and without intermittent oxide etching. During condensation process with intermittent silicon oxide etching, the formation of an undesirable amorphous SiGeO is observed. This is due to uncontrolled oxidation of silicon when the oxide layer is etched away. In the case of Ge condensation process without oxide etching, the authors could achieve a SiGe layer with 91% Ge concentration. A crystalline SiGeO layer at the interfaces of the top silicon oxide and buried oxide with SiGe was also observed. Possible formation mechanisms of amorphous and crystalline SiGeO are presented. Ge condensation process without SiO_2 etching utilizes four steps of oxidation and intermittent annealing cycles at each temperature resulted in $Si_{0.09}Ge_{0.91}OI$ substrate. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2432252]

SiGe-on-insulator (SGOI)-based templates are promising for mobility enhancement in strained channel metal-oxide semiconductor field effect transistors.[1] Ge condensation technique is being used to fabricate SGOI and Ge on insulator.[2,3] This technique employs oxidation of epitaxially grown SiGe on silicon-on-insulator (SOI) substrate wherein Ge atoms from SiGe are condensed into SOI to form a SGOI layer. The SGOI fabrication by condensation method is potentially attractive for the industry provided there is a clear understanding of the origin and mechanism of problems faced during the condensation process.[4] For a well controlled condensation process the challenge is to optimize the initial Ge concentration, the combination of oxidation/annealing process parameters such as temperature, pressure, and time and their effects on the condensation process will facilitate SGOI fabrication with required strain. In our earlier reports, a Ge condensation process with two-step oxidation was introduced to avoid the Ge balling up issue and SGOI amorphization.[5,6] This letter presents and compares two Ge condensation methods, one with and the other without intermittent oxide etching step to realize high Ge concentration SGOI. We address the mechanism of amorphous/crystalline SiGeO formation with/without intermittent SiO_2 etching during the Ge condensation. We discuss an optimized process flow which yields uniform SGOI with 90% Ge concentration. We also present the strain characterization results for the condensed SiGe layer.

About 120 nm thick $Si_{0.85}Ge_{0.15}$ film was epitaxially grown on a SOI substrate composed of 35 nm Si overlayer using an ultrahigh vacuum chemical vapor deposition technique. A Ge condensation process consisting of dry oxidation and annealing of SiGe was carried out at 1050 °C until a SiGe layer with Ge content of 60% was formed. Condensation experiments were further carried out with and without intermittent silicon oxide etch. In the case of oxide etched samples, the oxide was removed by dilute hydrofluoric acid. The Ge profiles were obtained by energy dispersive x-ray spectroscopy (EDS). The surface roughness of the SGOI layers was measured using atomic force microscopy. The crystallinity of the films was studied by cross-sectional transmission electron microscopy (XTEM) while micro-Raman measurements were performed to determine the strain state of SGOI.

Figure 1 shows the schematics of two Ge condensation process flows used to fabricate the SGOI substrate. Figures 1(a) and 1(b) show the first approach of Ge condensation process, with intermittent SiO_2 etching process, and Figs. 1(a) and 1(c) depict the second approach, without intermittent SiO_2 oxide removal between condensation steps. In the first approach, we carried out initial cyclic oxidation (3 cycles) at 1050 °C for 3 h with an intermittent annealing time of 30 min. After this, the oxide was removed and fur-

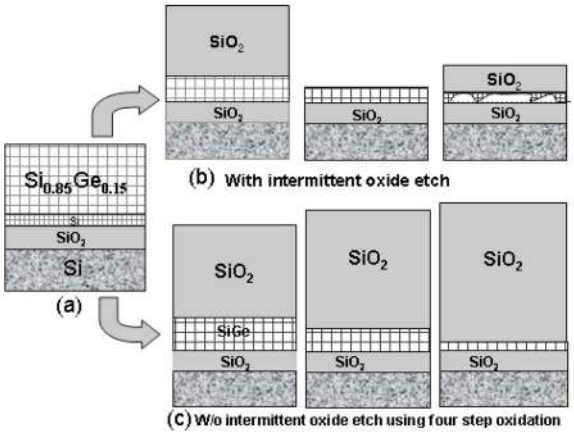

FIG. 1. (Color online) Schematic process flows of SGOI condensation with and without intermittent oxide etch: (a) As deposited, [(b) and (c)] flow with and without oxide etch, (d) overoxidized due to uncontrolled oxidation, and (e) high Ge content SGOI layer formed from controlled oxidation.

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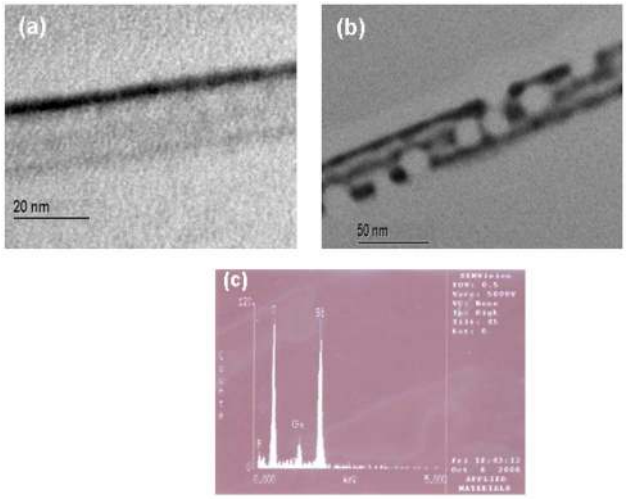

FIG. 2. (Color online) TEM images of layers (a) overoxidized at 1000 °C, (b) overoxidized at 925 °C showing SiO and SiGeO layers, and (c) EDS spectrum of SiGeO layer.

ther oxidation was carried out at 1050 °C for 2.5 h. It was found that up to 60% of Ge can be condensed at this temperature. The surface oxide was etched to avoid the self-limiting oxidation which was reported earlier.[2,7] Tezuka *et al.*[2] showed that oxidation is self-limited because the oxygen radical could not pass through the strained oxide layer. As explained by the model proposed by Shiumra *et al.*,[7] the self-limiting oxidation is also due to the melting of an interfacial layer having a high Ge concentration between the oxide and the SiGe layers. As the oxidation progresses, the Ge concentration in the film below the surface oxide layer increases. According to the phase diagram of the Si–Ge system, the interfacial layer melts when the concentration becomes more than 80% for the oxidation at 1000 °C. The interfacial layer is a mixture of liquid and solid phases having Ge concentrations of around 80%. Assuming that the mixed layers separate into liquid and solid, the oxidation rate would rapidly decrease since the Si concentration is very low at the oxidized interface. Ge diffusion would also be suppressed because the liquid and solid layers are stable at 1000 °C. We found that the intermittent oxide of SiGe removal enhances the oxidation rate; however, it is difficult to control the oxidation rate beyond 60% Ge concentration, achieving a minimal lateral nonuniformity less than 2%. Further oxidation was carried out at 1000 and 950 °C for the wafers. This oxidation process oxidized the entire SiGe layer for both the wafers. The TEM cross sections of the wafer along with EDS analysis are shown in Figs. 2(a) and 2(b), respectively. Though the oxidation temperature is lower as compared to the first oxidation at 1050 °C, the SiGe layer is fully oxidized since there is a higher diffusion rate of Ge in $Si_{0.4}Ge_{0.6}$ as the Ge diffusion coefficient increases with the increase of Ge content in the parent SiGe layer. We observe the formation of a layer of SiGeO for both the wafers. At the initial stage of oxidation, selective oxidation takes place and Ge further condensed which reduces the melting point of the SiGe layer and it enters into a semisolid state. Further arrival of oxygen radicals oxidizes this metastable layer converting it into a SiGeO layer as selective oxidation of Si over Ge does not take place since oxygen can easily diffuse through the plasma (metastable) state of SiGe, but difficult if through the solid form. Figure 2(a) indicates that at 1000 °C, SiGe is fully oxidized into the SiGeO layer while at 950 °C [Fig. 2(b)] the multilayer of SiGeO and crystalline SiGe with different germanium contents is observed. This can be due to the lower oxidation rate of SiGe at 950 °C as compared to that at 1000 °C. EDS analysis showing the presence of silicon mono-oxide (SiO) also points to a mechanism which indicates incomplete oxidation of Si at 950 °C. Figure 2(c) shows EDS analysis of oxidized layer among observed Ge, Si, and O elements in which oxygen content is more as it formed with Si and Ge. This confirms that the intermittent surface oxide removal during the oxidation steps has a significant impact on the Ge condensation process even at lower temperature (900–950 °C).

Based on the above analysis, a possible solution to increase the Ge content in the condensation process is to lower the oxidation rate. We can achieve this by lowering the oxidation temperature and reducing O_2 flow rate or by having a SiO_2 layer above the SiGe layer [Fig. 1(b)]. Lowering of temperature will reduce the Ge diffusion rates and accumulations of Ge can cause amorphization of SiGe lattice as reported in our earlier work.[6] Keeping a SiO_2 layer on top followed by condensation is expected to be more effective in controlling the further oxidation process. This is because oxygen radical diffusion gradually decreases with increased thickness of oxide layer during the process, and Ge diffusion is significant in SiGe with the temperature.[7–9] This allows more Si to be available to react with O_2 arriving at the oxide/SiGe interface and hence prevent O_2 diffusion deeper into the SiGe layer to form any SiGeO. Cyclic oxidation at 1050 °C for 1 h and annealing of 45 min (6 cycles) results in a uniform SGOI layer with 60% Ge concentration. It is a robust process to obtain SiGe with high Ge content as compared to the first approach of SiGe condensation with intermittent oxide etching. The surface roughness of SiGe was about 0.6 nm. Based on the phase diagrams, it is not advisable to continue the oxidation at 1050 °C for Ge concentration greater than 60% due to the formation of metastable SiGe layer.[7,8] Therefore, the oxidation temperature was reduced to 1000 °C for 30 min. We obtained a SGOI layer with 75% Ge using this two-step process. Further oxidation at low temperatures of 950 and 900 °C for 30 min each and with an intermittent annealing cycle of 30 min, we obtained 191 Å thick SGOI layer with 91% Ge.

A few undesirable issues were observed during the second and third oxidation steps carried out below 1000 °C. The schematic illustration of such issues observed at the SiGe oxide interfaces and the representative XTEM images are shown in Figs. 3(a)–3(d). A thin crystalline layer was observed in between the thermal oxide and SiGe with significant amount of oxygen. This is clear from the XTEM and EDS analyses of the wafer as shown in Fig. 3(c). We propose the mechanism for this undesirable consequence. During the oxidation, Ge accumulates at the top interface and is pushed down during annealing. As Ge diffusion in SiGe layer increases with increase of Ge content, the top portion of the layer enters into a metastable region (mixture of solid and liquid).[7,8] At that point, oxygen is absorbed by SiGe to reduce the interfacial free energy and to stabilize the solid phase which is a crystalline SiGeO as shown in Fig. 3(b). The inset in Fig. 3(b) shows distinct interfaces between SiGe and the layer. It is 3–5 nm thick SiGeO. Such a thin SiGeO layer formation can be eliminated by further annealing which pushes the Ge down and the SiGeO film will be converted to

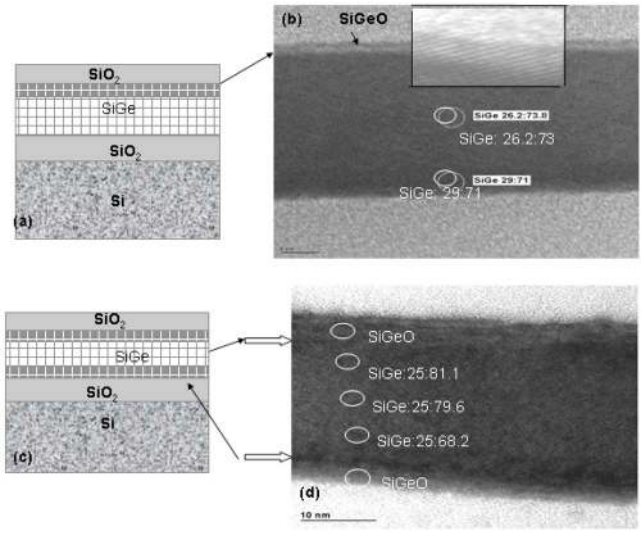

FIG. 3. (Color online) (a) Schematic of additional crystalline silicon germanium oxide (SiGeO) with SGOI. (b) TEM image of SGOI layer with additional layer at SiGe and top oxide. Inset shows the crystalline nature of the layer. (c) Schematic of double layers observed in SGOI layer. (d) TEM images showing the SiGeO oxide on both sides of the SiGe layer.

SiO_2. If this layer is thick, it may not be possible to completely remove it during the annealing process and as a result some defects will be formed at the interfaces. We overcome this problem by dividing the oxidation at four temperatures (1050–900 °C) as discussed earlier. During oxidation at 1000–900 °C, though the oxidation time was only 30 min at each stage, it was split into three steps. The oxidation was carried out for 10 min at each step with 30 min intermittent annealing for every oxidation to avoid the Ge accumulation at the interface and to improve the uniformity. This helps achieve SGOI with 91% Ge content and its XTEM is shown in Fig. 4(b).

Furthermore, during the oxidation at 950 °C when the Ge concentration increased from 75% to 80%, it was observed that the Ge content at the center of the condensed layer is higher than at the edges. The defective layers were also observed at both of the oxide/SiGe interfaces including the SiGe–buried oxide (BOX) interface as schematically shown in Fig. 3(c). Figure 3(d) displays the cross section TEM and EDS analyses indicating the presence of oxygen. The two arrows represent the observed interfacial SiGeO layers between SiGe and the oxide. Further oxidation may lead to oxidation of the entire layer. Multistep oxidation with more intermittent annealing at various temperatures used in this approach prevents SiGeO layer formation at the top oxide/SiGe and SiGe/BOX interfaces. The temperature should be carefully chosen well below the metastable region. The number of oxidation and annealing cycles depends on Ge concentration in the SiGe layer and should be increased with increase in Ge concentration.

We also investigated the lattice strain in SGOI using micro-Raman spectroscopy. Spectra for SGOI samples with Ge contents of 60% and 90% are shown in Fig. 4(c). In

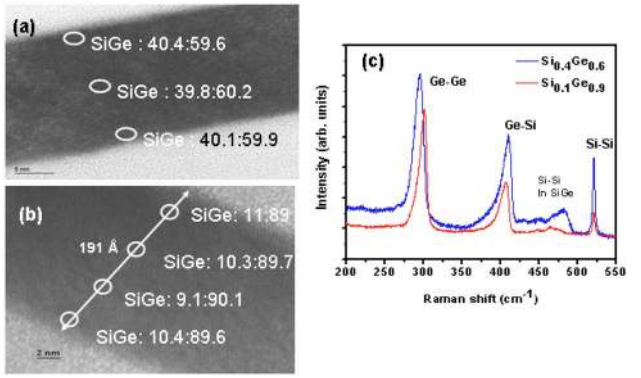

FIG. 4. (Color online) TEM images of (a) $Si_{0.4}Ge_{0.6}OI$ layer and (b) $Si_{0.10}Ge_{0.90}OI$ layer. (c) Raman data for the SGOI layers with 60% and 90% Ge.

Ge-rich $Si_{1-x}Ge_x$ films with Ge composition $x>0.5$, the strain is directly calculated from the frequency shift of Ge–Ge mode with respect to the phonon peak of bulk (strain-free) SiGe with the same Ge composition.[10] The average in-plane strain component that was calculated from such peak shift is 0.3% compressive for 60% Ge in SGOI and 0.5% compressive for 90% Ge in SGOI. The spectra also show the disappearance of Si–Si mode from SiGe when Ge content in SGOI increases above 90%.

In summary, we have investigated the effects of intermittent oxide etching on Ge condensation process for the realization of high Ge content SGOI. The Ge condensation without intermittent oxide etching gives better control on oxidation. Furthermore, single or dual SiGeO layer formation is evident at the SiGe and oxide interfaces after the condensation. This is an undesirable consequence and occurs when oxidation temperature falls near the metastable region of SiGe film. Utilizing a multistep Ge condensation process with frequent intermittent annealing process, nearly relaxed $Si_{0.09}Ge_{0.91}OI$ layers can be achieved without any undesirable SiGeO formation using the condensation technique without intermittent oxide etching.

[1]T. Mizuno, N. Sugiyama, T. Tezuka, T. Numata, T. Maeda, and S. Takagi, **50**, 988 (2003).
[2]T. Tezuka, N. Sugiyama, T. Mizuno, M. Suzuki, and S. Takagi, Jpn. J. Appl. Phys., Part 1 **40**, 2866 (2001).
[3]S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, Appl. Phys. Lett. **83**, 3516 (2003).
[4]V. Terzieva, M. Caymax, L. Souriau, and M. Meuris, ECS 2006 Abstracts, 209th ECS Meeting, Denver, CO, 7–12 May 2006, p. 17.2.
[5]M. M.-Roy, A. Agarwal, S. Balakumar, A. Y. Du, A. D. Trigg, R. Kumar, N. Balasubramanian, and D. L. Kwong, Electrochem. Solid-State Lett. **8**, G164 (2005).
[6]S. Balakumar, G. Q. Lo, C. H. Tung, R. Kumar, N. Balasubramanian, D. L. Kwong, C. S. Ong, and M. F. Li, Appl. Phys. Lett. **89**, 042115 (2006).
[7]T. Shiumra, M. Shimizu, S. Horiuchi, H. Watanabe, K. Yasutake, and M. Umeno, Appl. Phys. Lett. **89**, 111923 (2006).
[8]*Binary Alloy Phase Diagram* (American Society for Metals, Metals Park, OH, 1986), Vol. 2, p. 1248.
[9]Z. Di, P. K. Chu, M. Zhang, W. Liu, Z. Song, and C. Lin, J. Appl. Phys. **97**, 064504 (2005).
[10]P. H. Tan, K. Brunner, D. Bougeard, and G. Abstreiter, Phys. Rev. B **68**, 125302 (2003).