Received July 13, 2020, accepted July 30, 2020, date of publication August 10, 2020, date of current version August 21, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3015315

Control Strategies and Power Decoupling Topologies to Mitigate 2ω-Ripple in Single-Phase Inverters: A Review and Open Challenges

ADITYA R. GAUTAM[1,2], (Member, IEEE), DEEPAK M. FULWANI[2], (Member, IEEE), RAMMOHAN R. MAKINENI[2], AKSHAY KUMAR RATHORE[3], (Senior Member, IEEE), AND DHEERENDRA SINGH[1], (Senior Member, IEEE)

[1]Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science, Pilani, Pilani 333031, India
[2]Department of Electrical Engineering, IIT Jodhpur, Jodhpur 342037, India
[3]Department of Electrical and Computer Engineering, Concordia University, Montreal, QC 55104, Canada

Corresponding author: Deepak M. Fulwani (df@iitj.ac.in)

This work was supported in part by the DST-SERB-Core Research Grant, and in part by the Ministry of Electronics and Information Technology, Government of India.

ABSTRACT This paper provides a comprehensive review of the control approaches and the power-decoupling topologies to mitigate 2ω-ripple problem in the single-phase inverters, its solutions, and discusses open challenges yet to be addressed. The cause and effects of 2ω-ripple problem and its solution based on the passive and active power-decoupling techniques are discussed. A subcategory of the active power-decoupling technique nominated as the control-oriented compensation technique is reviewed in detail, this technique can achieve the ripple-mitigation at the source through the control but not necessarily adds extra circuit or active filter to the system. The control-oriented compensation techniques can be applied in the two-stage DC-DC-AC converters and the single-stage inverters having a front-end control capability with the H-bridge such as in the quasi-switched-boost inverters. The merits and associated challenges of these techniques are listed and summarized in a tabular form. Finally, a conclusive discussion with open challenges is presented.

INDEX TERMS 2ω−ripple, single-phase inverter, control strategies, power-decoupling schemes.

I. INTRODUCTION

Power converters are one of the important entity in the power applications such as renewable/hybrid energy applications, and the power inverters are generally used to supply AC loads in such applications. In the low power applications ($< 5\,kVA$), the single-phase power converter are generally used [1]. In the literature, several topologies of the single-phase DC-AC power converters, for example, Z source inverter (ZSI), quasi-ZSI, quasi-switched boost inverter (quasi-SBI), differential inverters, and two-stage converters are extensively explored for different power applications.

The DC-AC power converters supply to AC loads with the unwanted reflection of Second-order Harmonic Current SHC) ripple (2ω−ripple or two-time-line frequency ripple) at the DC input. In the single-stage DC-AC converter, this ripple at the DC link propagates towards the DC source and injects into the DC source if the DC link capacitance is not sufficient or no compensation technique is used. The 2ω-ripple poses same problem to the three-phase DC-AC converter with the unbalanced load condition [2]. The ripple also reflects in AC-DC power conversion [3]. A general practice to avoid the injection of ripple into the DC source is to use a large size aluminum electrolytic capacitor (E-cap) at the DC-link. However, the E-caps are vulnerable to low-frequency ripple due to low ripple handling capability and high parasitic resistance [4]. The ripple causes i^2r-heating loss inside the electrolytic capacitors [5], [6]. The life-span of an E-cap is $10\% - 90\%$ of a year at 105° C [4]; quite smaller than the life of a solar PV panel ($\approx$ 20 years) in a PV system [7]. This raises an important question on the reliability of complete system. A study conducted using data of 213 failure cases from 103 grid-tied solar PV systems at the Florida solar energy suggests that 139 failures are due to the inverter failure [8]. As per a study conducted in [9], in the power converters, 51% instances of inverter's failure are due to solid-state devices and aluminum capacitors. Moreover, 21% failure instances out of 51% are due to the aluminum capacitor failures only. The film capacitor is a reliable alternative to replace the electrolytic capacitor. The low ESR

The associate editor coordinating the review of this manuscript and approving it for publication was Shihong Ding.

value and large ripple handling capability of film capacitor makes it a suitable choice. However, an equivalent size of film capacitor is required in lieu of the electrolytic capacitor. The relative high cost of the film capacitor poses challenges to its viability [10]. However, the use of film capacitor is suitable and preferred in the active power decoupling circuits or control-oriented power decoupling techniques; a comparatively small size film capacitor is required in the active filter [11].

This paper reviews several power-decoupling techniques majorly classified as passive power-decoupling techniques (PPTs) and active power-decoupling techniques (APTs). Generally, APT adds additional power electronics circuit with an energy storage element such as film capacitor to the H-bridge. A subcategory of APTs, nominated here as the control-oriented compensation techniques (CCTs) for the two-stage DC-DC-AC power converters and single-stage inverters having front-end control-circuits with H-bridge such as in the quasi-switched boost inverters is discussed in detail. The CCTs eliminate the necessity of additional active filter. It is to be noted that the available review work in the literature [12]–[14] documents several active filter topologies to mitigate 2ω-ripple problem, however, this paper complements the available review work by providing a comprehensive review on the control-oriented techniques based on the different control strategies. The power decoupling-techniques are further categorized based on the topographical arrangement of active filter and control strategies i.e. application of power decoupling technique at (i) DC side of inverter and (ii) AC side of inverter (mixed-type). Beginning with the introduction of 2ω-ripple problem, the effect of SHC ripple on the system will be discussed. A detailed review of different 2ω-ripple mitigation techniques will be discussed. Eventually, the gaps and future scope are extracted and discussed. Section I begins with the introduction, followed by a discussion on the background of 2ω-ripple and its effect on the system in Section II. The Section III reviews several 2ω-ripple control schemes from the existing literature. In the Section IV, conclusive discussion and open problems are presented.

II. 2ω-RIPPLE: ITS BACKGROUND AND CONSEQUENCE

For an ideal inverter, the instantaneous values of input power and output power must be equal. However, in actual scenario, there is the power mismatch between the instantaneous values of DC power and AC power; the pulsating nature of AC power causes the pulsation in the DC input power.

A. BACKGROUND OF 2ω-RIPPLE

Suppose an inverter supplies AC load at ω rad/s. The mathematical representation of such systems is [15],

$$v_{ac} = V_m cos(\omega t), \quad i_{ac} = I_m cos(\omega t - \theta) \tag{1a}$$

$$v_{ac} i_{ac} = 0.5 V_m I_m cos\theta + \underline{0.5 V_m I_m cos(2\omega t - \theta)} \tag{1b}$$

$$p_{ac} = P_o + \underline{p_r} \tag{1c}$$

Here v_{ac} and i_{ac} are the instantaneous output AC voltage and output AC current of inverter. θ is displacement angle. The subscript m stands for the maximum value of v_{ac}/i_{ac}. The underline part of (1c) is 2ω-power ripple pulsating over the average DC offset. The Fig. 1(a) depicts this phenomenon.

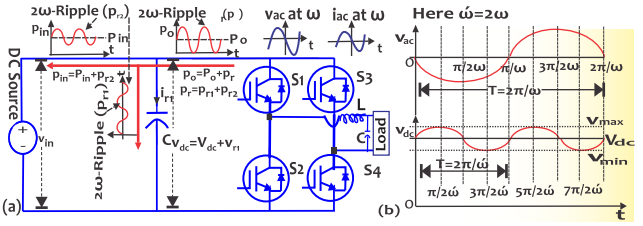

FIGURE 1. (a) Background of 2ω-ripple in single-phase inverter. (b) Waveform of AC output voltage and DC-link voltage.

In Fig. 1(a), suppose v_{dc} is the instantaneous voltage at DC-link and i_r is the current through DC-link capacitor (C) and assume 2ω-ripple passes through the capacitor only i.e. $p_r = p_{r1}$ and therefore no ripple propagates to the input i.e. $p_{r2} = 0$ then the instantaneous power of capacitor is,

$$p_r = v_{dc} i_r \tag{2a}$$

$$p_r = (V_{dc} + v_r) i_r = V_{dc} i_r + v_r i_r \tag{2b}$$

Here V_{dc} is the average voltage of DC-link and v_r is 2ω-ripple voltage. For large value of C, the value of v_r in (2b) is negligible, this implies that $v_r i_r \ll V_{dc} i_r$. This gives,

$$p_r = V_{dc} i_r \tag{3}$$

Using the value of p_r from (1c) in (3) gives,

$$i_r = \frac{0.5 V_m I_m cos(2\omega t - \theta)}{V_{dc}} = \frac{P_{rms} cos(2\omega t - \theta)}{V_{dc}} \tag{4}$$

Here *rms* stands for root-mean-square. Also,

$$i_r = C \frac{dv_r}{dt} \tag{5}$$

Using (4) and (5) gives,

$$dv_r = \frac{P_{rms}}{C V_{dc}} cos(2\omega t - \theta) dt \tag{6}$$

Integrating (6) from both sides and using upper and lower limits in it from Fig. 1(b) gives,

$$\int_{v_l}^{v_u} dv_r = \int_{\frac{\pi}{4\omega}}^{\frac{3\pi}{4\omega}} \frac{P_{rms}}{C V_{dc}} cos(2\omega t - \theta) dt \tag{7a}$$

$$\Delta v = v_u - v_l = \frac{P_{rms}}{2\omega C V_{dc}} [sin(2\omega t - \theta)]_{\frac{\pi}{4\omega}}^{\frac{3\pi}{4\omega}} \tag{7b}$$

$$\Delta v = \frac{P_{rms}}{\omega C V_{dc}} cos\theta \tag{7c}$$

Here Δv is the peak to peak voltage ripple and subscripts u and subscript l stand for upper limit and lower limit respectively. For the given value of Δv, P_{rms}, θ and V_{dc}, the size of capacitor required at the DC-link is,

$$C \geq \frac{P_{rms}}{\omega \Delta v V_{dc}} cos\theta = \frac{P_{rms}}{\omega \Delta v V_{dc}} p.f. \tag{8}$$

Here $p.f.$ stands for power-factor.

B. CONSEQUENCES OF 2ω-RIPPLE ON SYSTEM

The 2ω-ripple poses several issues related to cost, size, efficiency, reliability and stability on the system [16], [17]. This ripple forces an over-rated design of components and increases the peak-rating of system. Consequently, i^2r in the system increases. The i^2r-loss inside the E-cap causes heating of electrolyte [4], [18]. To restrict the DC-link voltage ripple to $\pm 1\%$, an E-cap of $\approx 6\ mF$ is required for a 100 W-inverter operating at 60 Hz with 48 V-DC-link voltage [19], the Fig. 2(a) depicts this issue. An injection of $2\omega-$ripple into the fuel cell causes fuel-starvation and stress on the membrane [20]. The low frequency ripples ($<400\ Hz$) should be kept $< 10\%$ for the long life expectancy [21], [22]. In [21], it is established that for a solid-oxide fuel-cell, a 17%-reduction in the peak-value of current ripple (from 22% to 5%) improves its efficiency by 5% that can go upto 9% for the ripple compensation by 31%. In PFC based LED lighting, the low frequency causes the flickering effect [19], [23], [24]. In the MPPT operation of the solar-PV or fuel cell, a pulsation of the $2\omega-$ripple about the maximum power points (MPPs) of the power/current/voltage may shift the actual MPPs. According to [25], a decrease of 5% in the efficiency and power of the solar-PV with MPPT operation is observed for an 8% ripple in the rms value of MPPs. In the Fig. 2(b), the effect of the $2\omega-$ripple on the MPPs is shown using P-V diagram [26]. Table 1 summarizes the Section II(B). The injection of 2ω-ripple into the battery causes heating effect. According to [28], a current ripple more than 8% may badly affect the electrodes and electrolyte of the battery and reduces the performance and efficiency of the system. Moreover, ripple increases the voltage/current stress on the system components [34], [35].

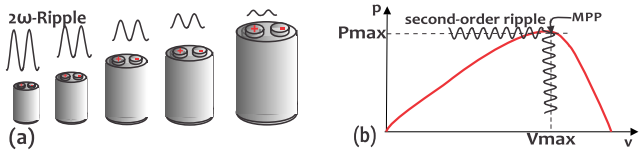

FIGURE 2. (a) For the same voltage rating, a large size E-cap decouples more 2ω-ripple. (b) Effect of 2ω-ripple on MPPT operation [27].

III. CLASSIFICATION OF RIPPLE MITIGATION METHODS

The propagation of 2ω-ripple towards the DC source can be avoided by storing the 2ω-power ripple in a large E-cap at the DC-link (at the input of inverter) or forcing the voltage to swing at 2ω directly at the DC-link itself or allowing the indirect voltage-swing across the film capacitor (other than at DC-link) through a power electronics based control. Besides this, the control-oriented techniques can directly be used in the two-stage DC-DC-AC converters and single-stage inverters with the front-end control-capability; this eliminates the necessity of additional active filter. Some control-oriented techniques are the output-impedance shaping, loop-bandwidth shaping in dual-loop control, generation of the ripple-free reference of the input current and forcing the ripple flow in the direction other than the DC source. In general, these different techniques can be classified as (i) passive power-decoupling techniques (PPTs) (ii) active power-decoupling techniques (APTs), and its sub-category (iii) control-oriented compensation techniques (CCTs) for inverter with front-end converter or in-built front-end control circuit. These techniques can be implemented (a) at DC side of the inverter and (b) at AC side of the inverter; a mixed-type arrangement. The Fig. 3 and Fig. 4 depict basic methodologies and control techniques of $2\omega-$ripple mitigation.

A. PASSIVE POWER-DECOUPLING TECHNIQUES

PPTs are conventional and easy to implement without using control schemes. The topologies shown in the Fig. 5(a-b) are the conventional stand-alone voltage source converter (VSC) [36]–[38] and grid-connected (VSC) [39]–[41] respectively.

Some of the isolated topologies are shown in the Fig. 5(c)-(d)-(f). A flyback-type center-tapped inverter (see Fig. 5(c)) is proposed in [42] for the isolated operation. The Fig. 5(d) shows a high frequency-link two-stage DC-DC converter for the high power applications [43], [50]–[52]. The converter shown in Fig. 5(e) can step-up/down voltage

TABLE 1. Summary of cause, effect and design constraint of $2\omega-$ripple.

Affected system/algorithm	Effect on system	Cause and constraint	Reference
Capacitor at DC-link	Heating effect; Reduction in life of aluminum capacitor by $10\% - 90\%$ a year at $105^o\ C$	Large ESR causes i^2r-losses and high temperature: a $10^o\ C$ rise in temperature, reduces life of E-cap by half; To limit voltage pulsation within $\pm 1\%$, a $\approx 6\ mF$ E-cap required for $100\ W, 60\ Hz-$inverter	[19], [28], [29]
Fuel cell stack	Poor efficiency and affect life	$2\omega-$ripple $> 10\% - 15\%$	[21], [22], [30]
Fuel cell MPPT	Excessive use of H_2/O_2 or reactant	$2\omega-$ripple $> 8\%$	[28]
Solar PV MPPT	Poor efficiency; Nuisance tripping	$2\omega-$ripple $> 10\%$; Oscillation about MPP	[25]
Battery	Affect the electrodes and electrolyte,	$2\omega-$ripple $> 8\%$; Heating due to hysteresis	[28]
LED lights	Flickering effect; Visual fatigue	No time delay or latency effect in LED lights against $2\omega-$ripple flicker should be restricted within 10%	[19], [24], [31] [23], [32]
System components	Over-rated design; High stress	low frequency and increase in peak values	[33]

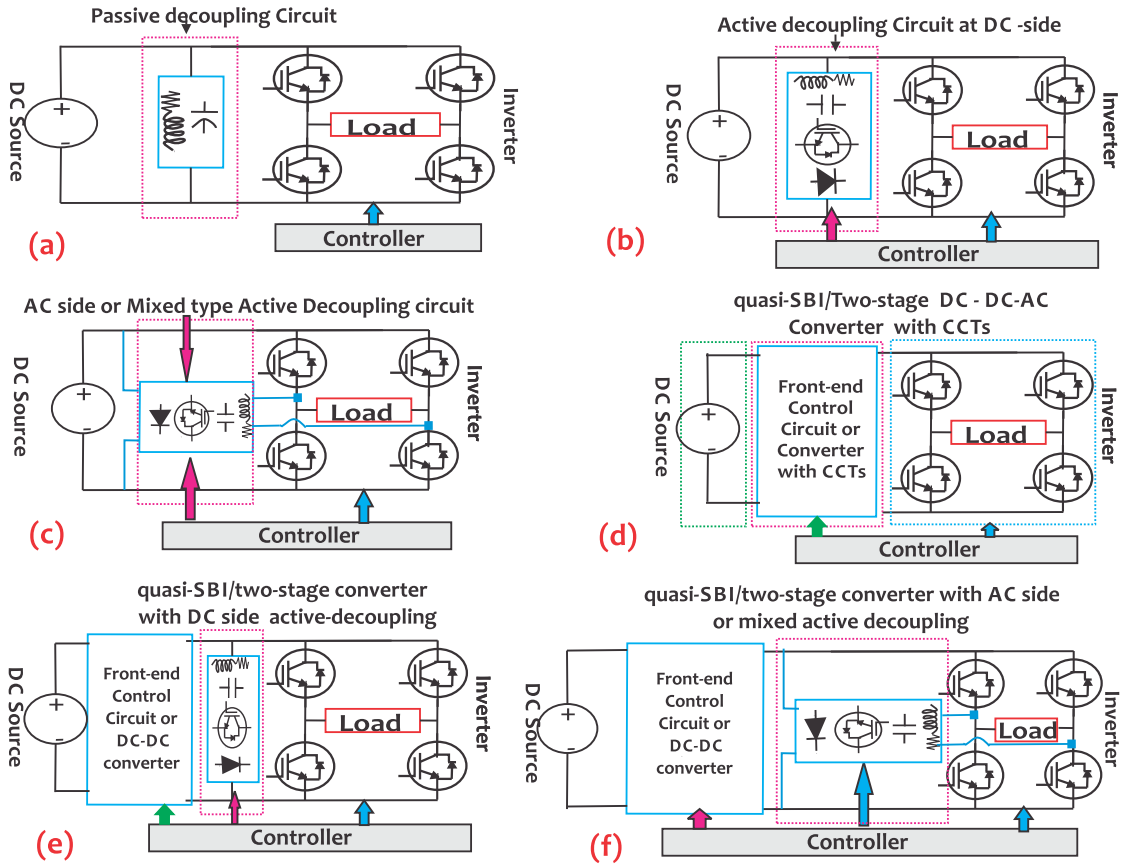

FIGURE 3. Topographical arrangements of power decoupling techniques: (a) PPTs at DC link (b) APTs at DC link (c) APTs at AC side; a mixed type arrangement (d) ZSI, quasi-SBI or two-stage DC-DC-AC converter with CCT only (e) ZSI, quasi-SBI or two-stage DC-DC-AC converter with active power decoupling circuit at DC side (f) ZSI, quasi-SBI or two-stage DC-DC-AC converter with mixed type active power decoupling circuit.

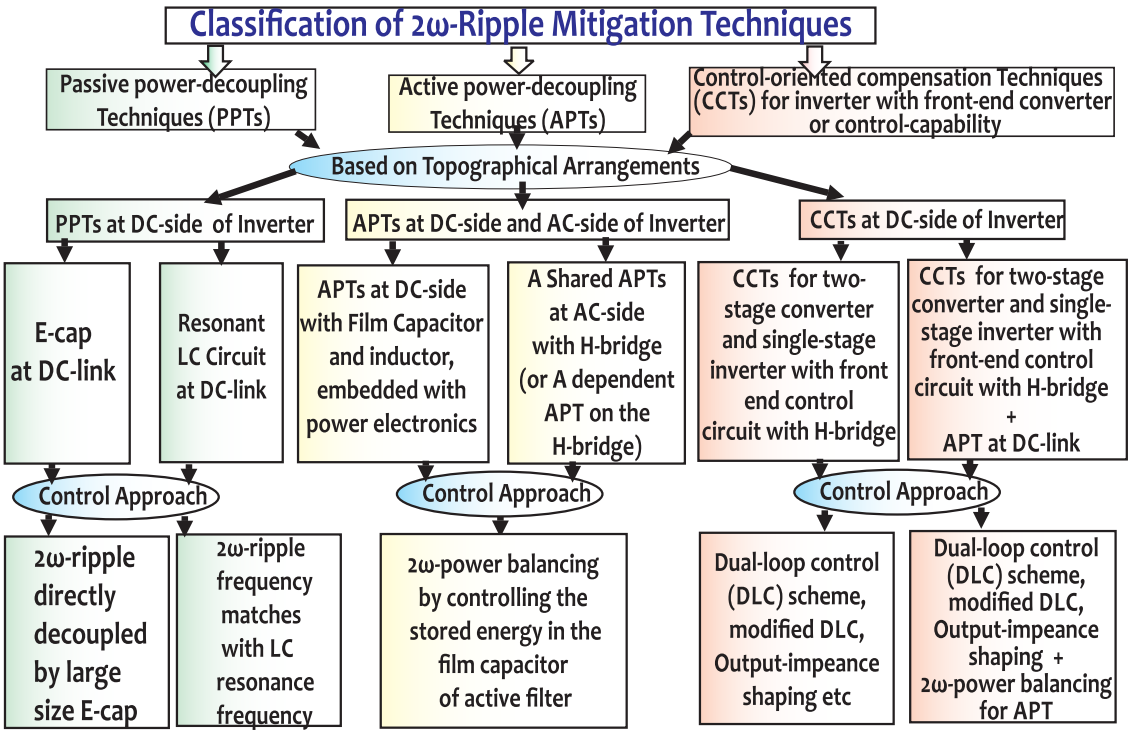

FIGURE 4. Flow chart of classification of 2ω−ripple mitigation techniques.

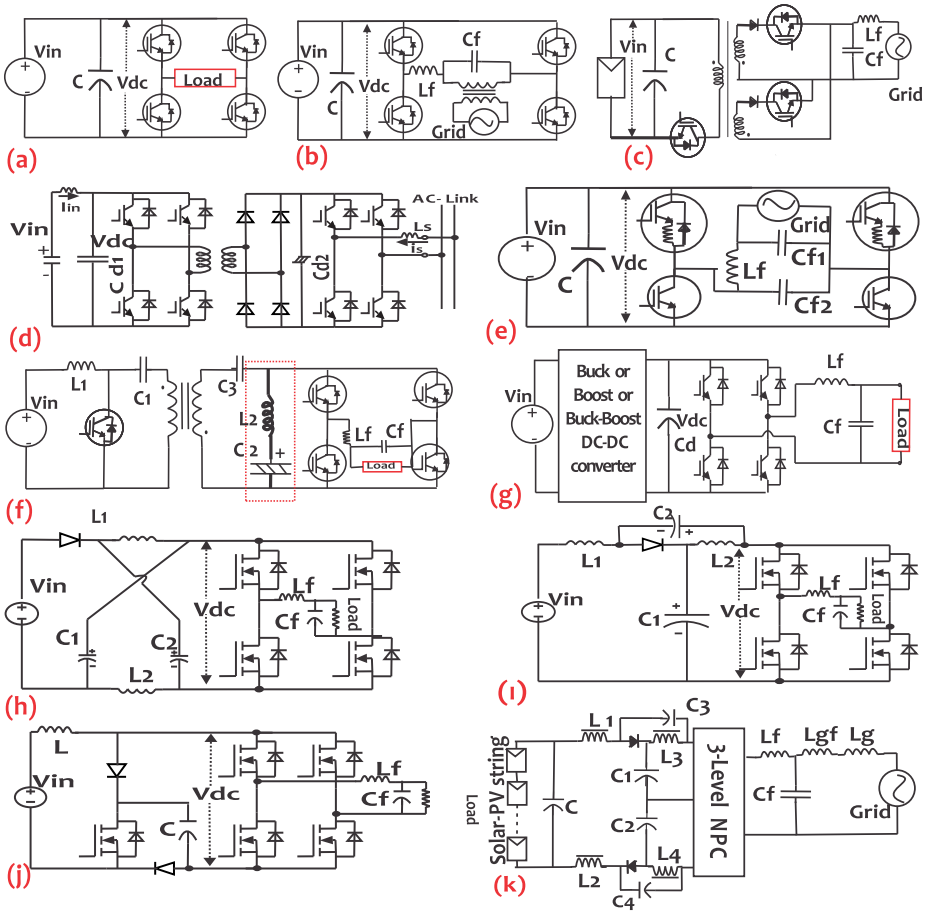

FIGURE 5. Passive power decoupling techniques. (a) Isolated Voltage source inverter [36]. (b) Grid-tied-Voltage source converter [39]. (c) Flyback-type center-tapped inverter [42]. (d) Inverter with front-end dual-bridge converter with high-frequency DC-link [43]. (e) Transformer-less buck and boost inverter topology [44]. (f) Pulse-link DC-AC converter [45]. (g) Two-stage DC-DC-AC converter (having a front-end buck or boost or buck-boost DC-DC converter) [46]. (h) Z-source inverter. (i) Quasi-Z source inverter. (j) Quasi-switched boost inverter. (k) Three-level single-phase impedance source inverter(Fig. 5(h-k) [47]–[49]).

without using a front-end DC-DC converter or a transformer [44]. All these topologies use a large electrolytic capacitor at the DC link [53]–[55]. The large size inductors used in the current-fed inverter can minimize the ripple at the input [56], and also by employing a tuned-resonant filter at the DC-link, the $2\omega-$ripple can be decoupled [57]. In [45], authors have proposed a pulse-link DC-AC converter (see Fig. 5(f)). In this topology L_2C_2 makes the resonating tank. This resonant-filter is tuned at 2ω such that the most of $2\omega-$ripple passes through the low impedance L_2C_2-branch when the resonance frequency (ω_o) matches with 2ω. The two-stage DC-DC-AC converter are popular in the RE energy applications [46], [58]–[60] (see Fig.5(g)). Conventionally, a large size E-cap is used at the DC link in these topologies. These topologies still have a challenge of accidental short-circuiting of the switches in the same leg(s) of the inverter [61]. The impedance-source inverters (ISIs) [47]–[49] are the good choice in such limitations and operating conditions. However, these topologies require large size impedance-source network to filter low-frequency $2\omega-$ripple [62]–[64]. In Fig.5(h-k), Z-source inverter, quasi-Z source inverter and quasi-switched boost inverter are shown.

B. ACTIVE POWER-DECOUPLING TECHNIQUES

Generally, APTs use additional power electronic devices and energy buffer especially a thin film capacitor. An inductor is also required to transfer 2ω-power ripple between the coupling point of active filter at the DC or AC side of the main circuit and the buffer capacitor connection point. The ripple control scheme is combined with the main control. In general, the control aims to balance the required 2ω-ripple power in the system by exchanging the reserved power of buffer capacitor in the active filter. Nevertheless, a proper selection of the film capacitor is a priori to keep the design optimum. The minimum size of the filter capacitor required in the different APTs is tabulated in the Table 2.

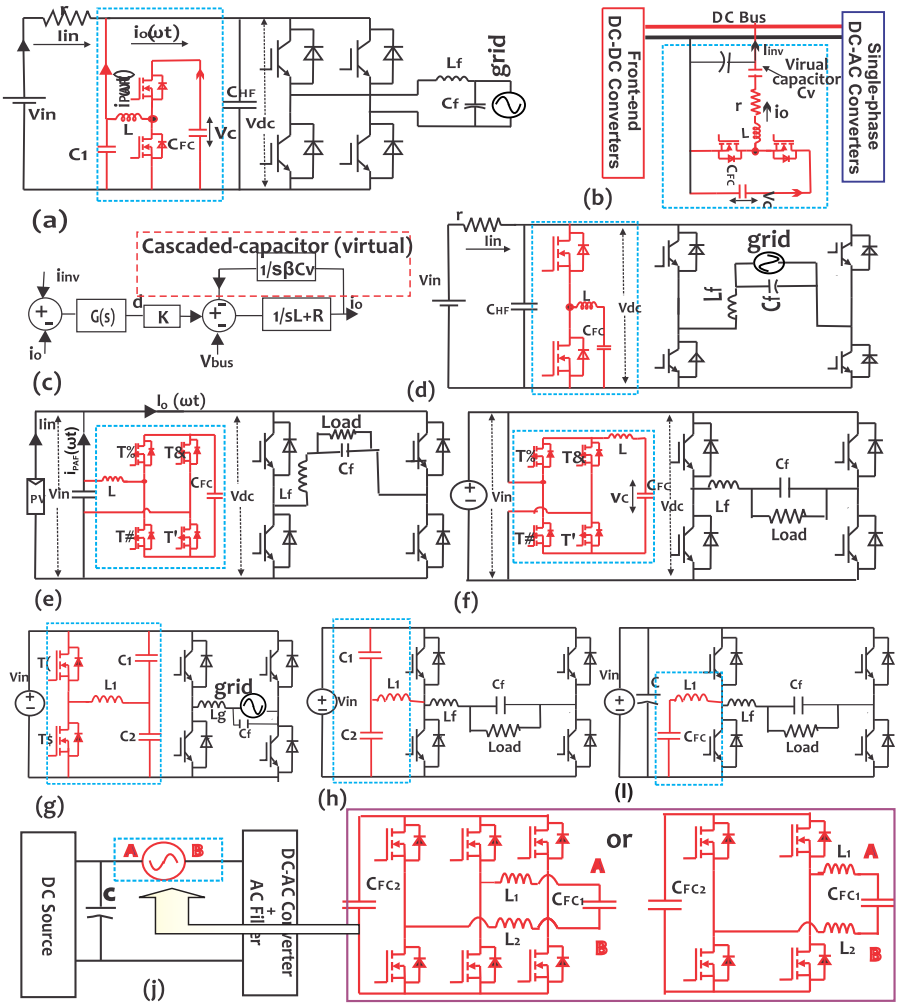

FIGURE 6. Active power-decoupling circuits at DC-link. (a) CPS-PAF-Boost type [65]. (b) ALFRCD with cascaded capacitor [66]. (c) Current control loop of ALFRCD with virtual cascaded capacitor [66]. (d) Bidirectional-buck type APT [67], [68]. (e) FB-RCR circuit [68], [69]. (f) Ripple-port circuit [19]. (g) Dual-voltage control decoupling strategy using a symmetric half-bridge circuit with H-bridge [70], [71]. (h) Dependent power decoupling with two-phase legs [1], [72], [73] and (i) [73], [74]. (j) Series power decoupling technique with two legs [75] and three legs [76].

1) APTs AT DC SIDE/LINK

In the DC side arrangement, the active power decoupling circuit is directly shunted at the DC-link by replacing the large size E-cap (see Fig. 6(a) to Fig.6(g).

These topologies are independent of the H-Bridge of the DC-AC power converter. The circuits in the Fig. 6(h) and Fig. 6(i) are the dependent decoupling circuits and utilize a part of the H-Bridge. Recently, some series power decoupling technique as shown in Fig. 6(j) are proposed [75]–[77]. This type of decoupling techniques add a series active decoupling circuit between the source and H-Bridge. In general, the active filter topologies are buck-type, boost-type, buck-boost type [65]–[67], [69], [78]–[81] and H-bridge type [19], [69], [82], [83], and the basic principle of ripple decoupling in the APTs using active filter (especially H-bridge type) at the DC-side is as follows [19]. Suppose C_{FC} is the film capacitor for power decoupling in active filter. The voltage across the film capacitor is v_c is given by,

$$v_c = V_{c_m} cos(\omega t + \varphi) \tag{9}$$

Here V_{c_m} is maximum value of the capacitor voltage and φ is an arbitrary phase-angle. The current through the capacitor is,

$$i_c = C_{FC} \frac{d}{dt} V_{c_m} cos(\omega t + \varphi) \tag{10}$$

The decoupling power ripple is given by,

$$p_{FC} = v_c(t) i_c(t) \tag{11a}$$

$$= v_c(t) C_{FC} \frac{d}{dt} V_{c_m} cos(\omega t + \varphi) \tag{11b}$$

$$= -0.5 C_{FC} V_{c_m}^2 \omega sin(2\omega t + 2\varphi) \tag{11c}$$

The 2ω-power ripple at DC-link is equal to p_{FC}. Applying power ripple balance at the DC-link and using (1cc)

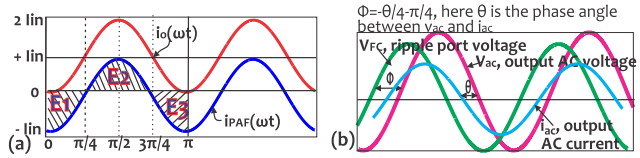

FIGURE 7. Working principle of (a) CPS-PAF [65], [69] (b) ripple port control [19].

and (11c),

$$0.5V_mI_mcos(2\omega t-\theta)=-0.5C_{FC}V_{c_m}^2\omega sin(2\omega t+2\varphi) \quad (12a)$$

$$P_ocos(2\omega t-\theta)=-0.5C_{FC}V_{c_m}^2\omega sin(2\omega t+2\varphi) \quad (12b)$$

In (12bb), the amplitude of V_{c_m} is adjusted by control such that $P_o = 0.5C_{FC}V_{c_m}^2\omega$ which follows,

$$sin(2\omega t+2\varphi)=cos(2\omega t-\theta) \quad (13)$$

Solving (13) gives,

$$\varphi=-\frac{\pi}{4}-\frac{\theta}{2} \quad (14)$$

The active filter decouples 2ω power ripple if (14) holds and $P_o = 0.5C_{FC}V_{c_m}^2\omega$ is satisfied by some value of V_{c_m}. The control adjusts φ and V_{c_m} to buffer 2ω-power ripple.

In [65], a current pulsation smoothing-parallel active filter (CPS-PAF) is proposed. The CPS-PAF consists of a small film capacitor and a conventional non-isolated buck/boost circuit (see Fig. 6(a)). This circuit behaves like a current-source. The working principle of power decoupling is shown in the Fig. 7(a) [65], [69]. In Fig. 6(a), the controller continuously compares the input current (I_{in}) with instantaneous value of the DC-link current ($i_o(\omega t)$). For $I_{in} > i_o(\omega t)$ in interval $0-\pi/4$ and $3\pi/4-\pi$, the capacitor C_{FC} stores energy (boost-mode) and for $I_{in} < i_o(\omega t)$ in interval $\pi/4-3\pi/4$ releases the energy (buck-mode). For energy stored (say E_1+E_3) equals to energy released (say E_2) by C_{FC}, the low frequency pulsation at the DC-link is zero. C_{HF} takes care of high frequency ripples. However, the active power imbalance between input and output of PAF and the power loss of PAF cause a decrease in the voltage of C_{FC} resulting in a lower value of V_c than the DC-link voltage. In such case the PAF gets short-circuit the input and output and ripple elimination is affected [69]. To resolve this problem, a mixed type APT version of CPS-PAF is proposed in [65] (see Fig. 9(f)). The grid feeds the rectified power to C_{FC} through the line transformer to compensate the losses. However, the system becomes bulky and complex. In Fig. 6(b), a buck-boost type active low-frequency ripple control device (ALFRCD) is shown that is proposed in [66] for the building-integrated photo-voltaic (BIPV) systems. The concept of ripple mitigation using ALFRCD is same as presented in [65]. However, in [66], a virtual capacitor is added in series with the inductor of the active filter through the control (see Fig. 6(b)). The virtual capacitor is realized by adding an integrator in the current control-loop (see Fig. 6(c)).

The control scheme forces the output current of the active filter (i_o) to track the DC-link current (i_{inv}). The important requirement of this scheme is to keep the voltage of the film capacitor (C_{FC}) higher than the bus voltage. Wang *et al*. proposed a similar bidirectional buck type-APT (see Fig. 6(d)) in [67]. The working principle of the power ripple decoupling control scheme is same as in [65] (see Fig. 7(a)). In [67], a DCM control scheme is used such that the C_{FC} stores all the $2\omega-$ripple and L functions like a power transfer element. Therefore, L does not store decoupling power that is good in terms of the power-density. Also, unlike CPS-PAF, the voltage of C_{FC} is less than the DC bus or DC-link voltage or any other voltage in the system. It is to be noted that the discontinuous current mode (DCM) operation of the front-end DC-DC converter of two-stage converter minimizes the input 2ω-ripple inherently due to the less interaction of DC source and DC-link during discontinuous operation [84]. The buck-derived and boost-derived two-stage converter has minimum $2\omega-$ripple at the input in the DCM operation. A four-switch based bidirectional full-bridge-ripple current reduction (FB-RCR) circuit is shown in the Fig. 6(e) [69], [75]. The working principle of the FB-RCR is same as of CPS-PAF of [65]. However, unlike [65], there is no requirement of the line-frequency transformer with the rectifier. The internal energy losses which are the cause of constant voltage decrease of C_{FC} in the FB-RCR circuit are compensated by sourcing power from the input source itself. However, the FB-RCR circuit contains four switches which operate at the high frequency. Therefore, the system becomes bulky and the switching loss increases. A similar APT based on the ripple-port concept is presented in [19] (see Fig. 6(f)). The control design is based on (9)-(14). The working principle of this technique is depicted in the Fig. 7(b). In the Fig. 6(f) and Fig. 7(b), ϕ is the phase difference between the instantaneous voltage of the film capacitor (v_{FC}) across C_{FC} and output voltage of inverter (v_{ac}), and θ is the displacement angle between instantaneous value of v_{ac} and i_{ac}.

In [70], Tang *et al*. have proposed a dual voltage control strategy for the symmetric half-bridge circuit with H-bridge. The circuit diagram is shown in the Fig. 6(g). The two capacitors (C_1, C_2) are used to decouple the power ripple. The control scheme aims to modulate the switches of half bridge such that the voltages across the two capacitors are equal and 2ω-pulsating voltage component over the offsets of voltages are out of phase by 180°. Following the power balancing condition, the required power decoupling condition is,

$$\varphi = 0.5tan^{-1}\left(\frac{-V_{rms}}{\omega L_f I_{rms}}\right) \quad (15a)$$

$$V_c = \sqrt{\frac{\sqrt{(V_{rms}I_{rms})^2+(\omega L_f I^2 m)^2}}{\omega(2C_f-L_f(2\omega C_f)^2)}} \quad (15b)$$

Here I_{rms} and V_{rms} are *rms* values of AC current and voltage. I_m is maximum current of AC current. $C_f = C_1 = C_2$. V_c is rms offset-voltage of capacitors. φ is phase difference between the grid voltage and pulsing voltage in the capacitor.

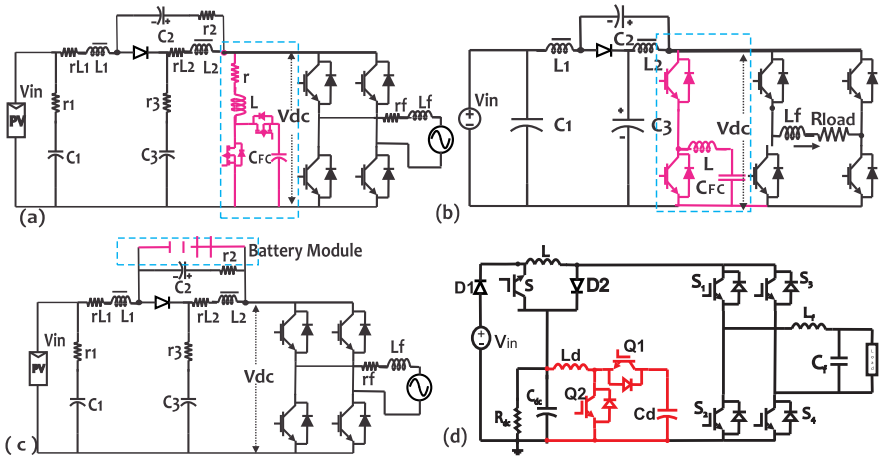

FIGURE 8. quasi-ZSI with DC-side (a) boost-type active filter [85] (b) bidirectional buck-boost type active filter [86] (c) battery module [87] and (d) boost-type APT [66] for single-phase switched boost inverter [88].

The active power decoupling techniques shown in the Fig. 6(h) and Fig. 6(i) share at least one of the phase of H-bridge and active filter. Therefore, such APTs are dependent on the H-bridge. This affects the modulation signal of inverter. In the two-phase legs topologies (see Fig. 6(h-i)), the DC voltage utilization is always kept $\leq$ 0.5 to avoid the over-modulation and to keep the size of film capacitor minimum.

In the impedance source inverters, the minimization of size of impedance network in the presence of $2\omega-$ripple is a challenge. In [85], a hysteresis current controlled active filter is proposed to confine 2ω-ripple within the active filter (see Fig. 8(a)). The control logic is same as shown in the Fig. 7(a). However, the ripple control design for the quasi-ZSI is somewhat more challenging than the H-bridge converter. A bidirectional buck-boost type active filter for quasi-ZSI is shown in the Fig. 8(b) [86]. The design of active filter is similar as shown in the Fig. 6(d). In [87], a comprehensive design of asymmetric ZS-network in the perspective of high frequency and low frequency ripple minimization is discussed the first time. The optimum design of ZS network is presented for a battery energy-stored quasi-Z source inverter (see Fig. 8(c)). A study on $2\omega-$power decoupling in switched boost inverter is carried out in [88] (see Fig. 8(d)). The boost-type APT proposed in [66] is used in this work. As discussed before, the E-cap is most vulnerable component, a pre-analysis of the effect of impedance network of quasi-ZSI and shoot-through duty on the remaining useful life of E-cap may help designers to predict the overall life of system [89].

2) APTs AT AC SIDE; A MIXED TYPE ARRANGEMENT

This arrangement of APT utilizes a part of DC side and a part of AC side of the main circuit, and the active filter generally shares atleast one leg of the inverter. The AC-side power decoupling techniques improve the power conversion efficiency in comparison to the DC-side power as the low frequency power pulsations are forced to confine at the AC-side [90], [91]. Some of recent AC side APTs are shown in the Fig. 9. In [1], Serban has proposed an APT using two decoupling capacitors at the AC-side (see Fig. 9(a)). The technique does not add extra power electronics to main circuit. However, the DC-link voltage and current loading of the inverter set a trade-off for the values of decoupling capacitors. Consequently, the efficiency of system is affected. The utilization factor of storage elements is $<$ 50%. The circuits of Fig. 9(b-g) add extra switches to the system. The inclusion of third leg with the H-Bridge reduces the stress on the switches by 57% in comparison to H-Bridge [93], [96]. Zhu *et al*. in [91] proposed a ripple confinement control technique for the circuit shown in Fig. 9(b). This technique implements a voltage waveform control [90] to confine the pulsating power within the capacitors at AC-side. A brief explanation of the waveform control is presented in the subsection III(D). A 100% utilization of the storage elements can be achieved using this method. However, this technique adds an extra pair of switches (see Fig. 9(b)) and increases the voltage-stress on the capacitors. In [92], Chen *et al*. have proposed a 2ω-power pulsation mitigation at the DC-link using the SVPWM method for the circuit proposed in [97] (see Fig. 9(c)). This technique eliminates capacitance and minimizes voltage and current stress on the switches for a range of the power factor. However, two extra switches are required and the total device power rating is increased by 50%. An APT for grid connected AC-DC power converter as shown in the Fig. 9(d) is proposed in [93]. This APT significantly reduces the size of DC-link capacitor. The stress on switches is reduced up to 70% for all the power factor. The study analyzes the effect of grid-side inductance as well and provides design guidelines for different system parameter for the practical implementation. Another APT is proposed in [94] for microinverter applications; a problem

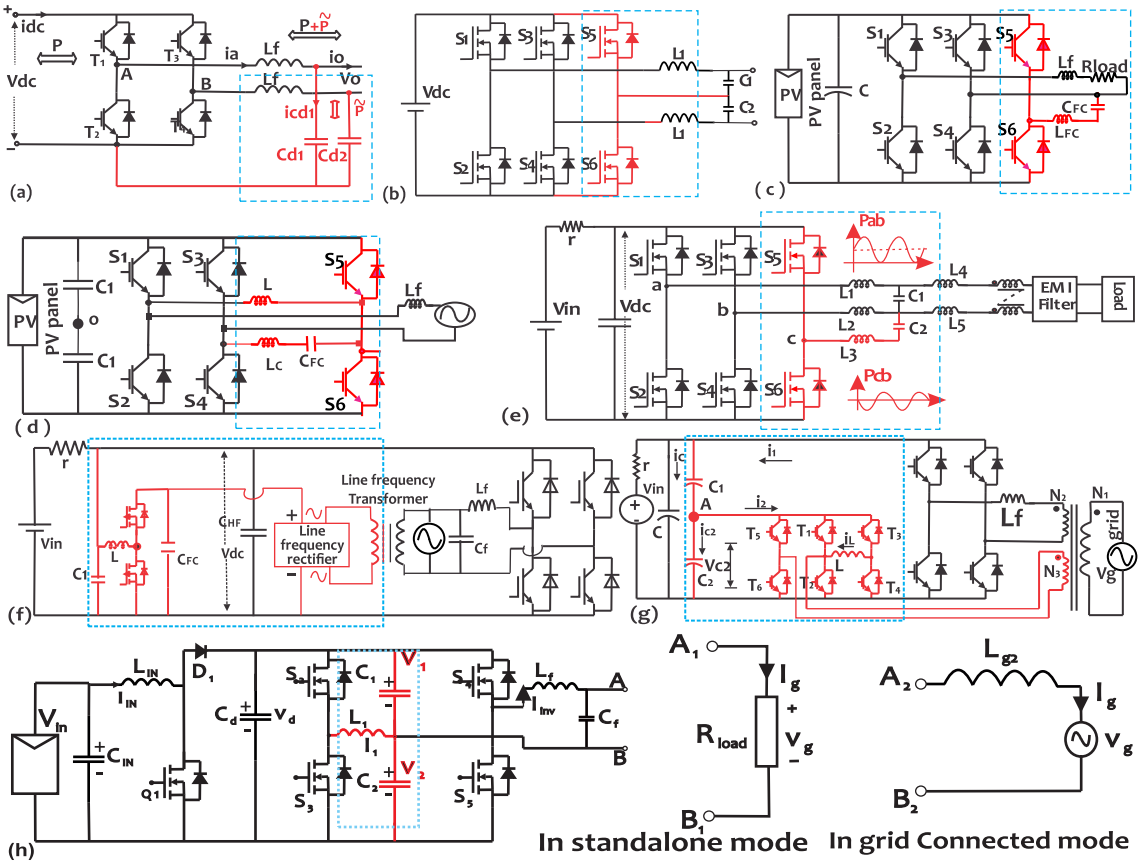

FIGURE 9. Mixed type of APTs without adding extra power electronics (a) proposed in [1] and adding extra pair of switches (b) proposed in [91] (c) proposed in [92] (d) proposed in [93] (e) proposed in [94] (f) Modified version of CPS-PAF scheme based circuit in Fig. 6(a) [65] (g) Hybrid filter [57] (h) proposed in [95].

from the Google little box challenge. The proposed technique is implemented on the GaN-based $3\phi-$inverter topology as shown in the Fig. 9(e). In the circuit of Fig. 9(e), the load is fed between the phase a and b and the decoupling circuit is placed between phase b and c. The basic principle of ripple cancellation is that the control keeps the sum of instantaneous powers p_{a-b} and p_{b-c} a constant value. Therefore, the ripple is confined within the AC side decoupling circuit and DC side becomes ripple-free. The GaN switches have comparatively better figure of merits such as low on-state conduction loss, wide-band gap, switching frequency and efficiency. A similar topology is presented in [97]. In [57], a hybrid filter is proposed as shown in Fig. 9(g). In the hybrid filter, there are three legs. The ripple energy is stored in both, capacitor C_1 and inductor, L. Using Kirchhoff's current Law at A in Fig. 9(g),

$$i_C = i_1 - (i_2 + i_{C2}) \tag{16}$$

In Fig. 9(g), for $C_2 \ll C_1$ the i_{C2} can be neglected in (16),

$$i_C \approx i_1 - i_2 \tag{17}$$

The hybrid filter generates i_2 such that $i_1 = i_2$. For this the inductor current is controlled to keep the voltage across C_2 constant. However, the voltage v_{c2} keeps on decreasing due to internal loss of filter. The hybrid filter alone is not sufficient. Therefore, an additional leg (switches T_5, T_6) is added to import the energy from the grid as shown in Fig. 9(g). This is a mixed type APT. Nevertheless, a small capacitor can be used for the power decoupling. However, the extra switches in third leg make the circuit bulky. In [95], authors presented a single-phase inverter topology that is a combination of front-end boost stage, a half-bridge inverter stage, and a buck–boost type power decoupling stage (see Fig, 9(h)). The size of decoupling capacitor used in this work is optimized based on efficiency of converter, average dc-link voltage, and dc voltage utilization factor of the capacitors.

An AC side active filter is proposed for the quasi-ZSI in [63]. The control confines 2ω ripple within the LC of filter using a third leg besides the H-bridge (see Fig. 10). The control aims to switch the third leg such that 2ω-ripple energy stored in L and C_{FC} of filter is exchanged; the power decoupling principle is same as presented in [19]. However, the energy stored in inductor is also considered. In Fig. 10, the decoupling ripple power between B and C is given by,

$$p_{FC} = v_c i_{FC} + L\frac{di_{FC}}{dt} i_c \tag{18a}$$

$$= \frac{V_{c_m}^2 C_{FC}(1 - \omega^2 LC_{FC}) sin2(\omega t + \varphi)}{2} \tag{18b}$$

TABLE 2. Design of minimum value of filter capacitor.

Topology or Filter type	Filter location	Minimum design value	Reference
1) E-Cap	DC-link at DC side	$C_{dc} = \frac{P_o}{\omega V_{dc} \Delta v}$	[19]
2) LC series filter (See Fig. 22(h))	Embedded with centre taping of transformer in half-active bridge in DC-DC-AC converter	$C_{FC} = \frac{P_{in}(P_{in} - V_{in} I_{trans})}{\omega V_c V_{in}(2P_{in} - V_{in} I_{trans})}$	[98]
3) LC filter in H-Bridge type active filter (See Fig. 22(f-g))	Embedded with active filter at DC side	$C_{FC} = \frac{2P_{in}}{\omega V_{cm}^2 (1-\omega^2 L)}$	[83]
4) Flying capacitor (See Fig. 23(f))	Flying capacitor in modified boost- derived DC-DC-AC converter	$C_{FC} = \frac{2W}{\omega(v_u^2 - v_l^2)}$	[81]
5) Extra third leg and LC filter with H-Bridge(See Fig. 10)	Embedded with active filter at AC side	$C_{FC} = \frac{4V_m I_m}{4V_m I_m \omega^2 L + V_{dc}^2 M_{32} \omega}$	[63], [99]
6) E-cap at DC-link	At DC-link of two-stage converter	$C_{dc} = \frac{1.359S}{\omega \Delta v V_{dc}}$	[59]
7) Capacitors and Inductors (See Fig. 5(i))	quasi-Z Source network	$C_1 = C_2 = \frac{(1-2D_{sh})^2 + \sqrt{(1-2D_{sh})^2 (\frac{V_m I_m}{2V_{dc} i_{Lr}})^2 - (\frac{4\omega L I_{dc}(D_{sh}-1)}{V_{dc}})^2}}{4\omega^2 L}$, $L_1 = L_2 = \frac{v_{cr}(1-2D_{sh})}{2\omega i_{Lr}}$	[62]
8) E-cap at DC-link with control strategy proposed in [100]	E-cap at DC-link of two-stage converter	$C_{dc} = \frac{2T_{ac}\Delta P}{\Delta v(2V_{dc} + \Delta v)}$	[100]
9) Capacitors (See Fig. 20(d))	High gain q-SBI Network	$C_1 = \frac{D_{sh}(1-D_{sh})(1-2D_{sh})}{2v_1 \%(1-4D_{sh}+2D_{sh}^2) f R_L}$, $C_2 = \frac{(1-D_{sh})^2}{2v_2 \%(1-4D_{sh}+2D_{sh}^2) f R_L}$	[101]
10) CPS-PAF (See Fig. 6(a))	Embedded with active filter at DC side	$C_{FC} = \frac{0.422\pi P_{in}}{\omega(V_u^2 - V_l^2)}$	[65]
11) LC filter (See Fig. 23(e))	Embedded with the main circuit at AC side	$C_{FC} = \frac{V_m I_m}{\omega V_c^2}$	[79]

In Table 2, Input power, P_{in}; input voltage, V_{in}; Peak to peak ripple voltage across C_{FC}, v; Upper voltage limit of v, V_u; Lower voltage limit of v, V_l; Average voltage across filter capacitor (C_{FC}), V_c; Maximum voltage across filter capacitor, V_{cm}; Transformer current, I_{trans}; maximum voltage/current at inverter output, V_m / I_m; DC-link voltage, V_{dc}; DC-link current, I_{dc}; Modulation index, M_{32}, series inductance with C_{FC}, L; Apparent output power of inverter, S; Peak-peak DC-link voltage ripple, Δv; Shoot-through duty, D_{sh}; Desired amplitude of 2ω-ripple in through inductor, i_{Lr}; Desired amplitude of 2ω-ripple across C, v_{cr}; Time period of AC output, T_{ac}, Power mismatch during T_{ac}, ΔP; Capacitors used in [101], C_1, C_2; Peak-to-peak voltage ripple (of C_1, C_2), v_1, v_2; Simplified equivalent DC load, R_L; switching frequency, f; angular supply frequency of inverter, ω, Buffer energy, W.

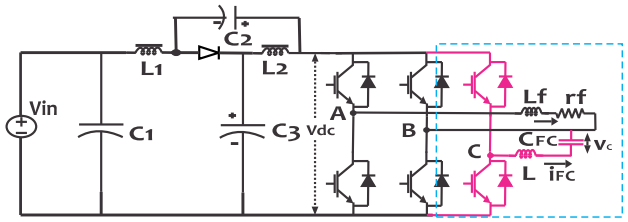

FIGURE 10. Mixed type active decoupling circuit for the quasi-ZSI [63].

To decouple the 2ω−power ripple, the addition of the 2ω−ripple power component of (1cc) and p_{FC} in (18bb) should equate to zero i.e. $p_r + p_{FC} = 0$. This implies,

$$P_o cos(2\omega t - \theta) = 0.5 V_{cm}^2 C_{FC}(1 - \omega^2 L C_{FC}) sin(2\omega t + 2\varphi) \tag{19}$$

Here V_{cm} is the maximum value of the voltage across the C_{FC} and i_{FC} is the current through L. $P_o = 0.5 V_{rms} I_{rms}$. To decouple the power ripple the control follows $P_o = 0.5 V_{cm}^2 C_{FC}(1 - \omega^2 L C_{FC})$ and $\theta = -0.5\varphi + \frac{\pi}{4}$.

Recently, a research has been conducted on high frequency ripple at source in the impedance source inverters [102], [103]. However, the focus of this review work is low-frequency ripple (2ω−ripple) hence effect of high frequency is not covered here.

C. CONTROL-ORIENTED COMPENSATION TECHNIQUES (CCTs)

Two-stage DC-DC-AC converters and single-stage DC-AC converters with front-end control capability can mitigate the ripple at input using the suitable control, this eliminates the necessity of active filter. The main concept is to design a control scheme that restricts the propagation of 2ω−ripple towards the DC source(s) while forcing the ripple to confine at the DC link. However, this causes a deliberated increase in 2ω-pulsation at the DC-link. This may affect the THD level of output of the inverter. According to European standards (EN50160) for the public distribution systems, the low frequency voltage pulsation of the DC bus-voltage should be kept within 2% range and the THD level of output of the inverter should be kept within 5% [104]. Therefore, an optimum design of the DC-link capacitor is involved. The ripple can be eliminated completely by using an active filter at the DC bus. The Fig. 11 shows block diagrams of the stand-alone and grid-connected DC-DC-AC converter with active-filter and without active-filter at the DC-link.

1) CCTs WITHOUT ADDITIONAL ACTIVE FILTER

Kwon *et al.* have proposed a current-fed resonant push-pull converter and DC-AC converter based power conditioning system (PCS) for the fuel-cell application

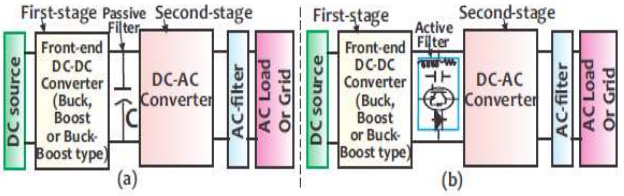

FIGURE 11. Two-stage DC-DC-AC converter. (a) Stand-alone/Grid-tied without active-filter. (b) Stand-alone/Grid-connected with active-filter.

with a ripple-mitigation compensator [34]. The control block-diagram is shown in the Fig. 12(a). The control generates a duty (D_o) for the DC voltage regulation in the closed-loop. A feed-forward controller takes care of the $2\omega-$ripple by adding ripple-cancellation duty (D_r) to D_o. To reduce the ripple further, a perturbed duty (ΔD) is generated using the current control-loop and added to give overall duty ($D = D_o + D_r + \Delta D$). However, the performance of the feed-forward controllers are poor in terms of disturbance rejection and robustness against parametric uncertainty [105]. Feedback control approaches are widely used in the different applications such as tracking, regulation, disturbance rejection, robust control. In literature, the concept of the ripple-mitigation using the feed-back control in the two-stage converters is put forward in the two perspective. First one is based on the adopting a modified dual-loop control method. The method utilizes a current mode control (CMC) scheme. Second method is based on the output-impedance shaping. The method of output-impedance shaping can be implemented in a voltage mode control (VMC) i.e. using a single control loop also.

The CMC-based dual-loop control method has an inner current-loop and an outer voltage-loop. To ensure the ripple-reduction at the input of the two-stage converter, the interaction between the inner-loop and outer-loop is avoided such that disturbances in the voltage-loop do not pass to the current-loop [17], [105], [106]. One way to achieve this is to make a separate current-loop control and voltage-loop control as shown in the Fig. 12(b) [105]. However, in such schemes, the current-loop of the first-stage should be designed to get a very high gain at 2ω. This makes the real-time implementation challenging due to hardware limitations [105]. Liu and Lai have proposed a dual-loop control method for the front-end converter of a fuel-cell sourced DC-DC-AC converter [106]. The Fig. 12(c) depicts the dual-loop control method. The basic concept of the ripple reduction proposed in [106] is based on the bandwidth-shaping. Instead of making the independent current-loop and voltage-loop, the bandwidth (BW) of voltage-loop is reduced significantly. According to [106], a reduction in the $2\omega-$ripple at the input can be achieved provided that the BWs of inner-loop and the outer-loop have a separation of half-decade (at least) from 2ω frequency. The basic idea is the minimization of $2\omega-$ripple component in the reference current of the inner-loop controller. However, the very low BW of the voltage-loop causes the sluggish or poor system response at the load transients. Therefore, this method has a trade-off between the $2\omega-$ripple-reduction and dynamic performance. In Fig. 14, the effect of bandwidth of voltage-loop on the ripple-reduction and dynamic performance is depicted using simulation results. These results are presented for an $1 - kW$ boost-derived DC-DC-AC converter having input voltage, 120 V; DC-link voltage, 380 V; $L = 1\ mH$; $C = 360\ \mu F$ and AC voltage 230 V, 50 Hz. In Fig. 14, the f_v and f_c are cut-off frequencies/BWs of voltage-loop and current-loop respectively. G_{vd} and G_{cd} are control to voltage and control to current transfer functions. Tv and T_c are closed-loop-gains of voltage-loop and current-loop respectively. The results of Fig. 14 are summarized in Table 3.

Recently, 2ω-ripple problem is addressed in conjunction with the hybrid parameters of DC-DC converter. These parameters relate the input-output behavior of DC-DC converter. A general input-output relation using the hybrid parameters of two-port network (see Fig. 13) is given by [108],

$$\begin{bmatrix} \tilde{v}_o(s) \\ \tilde{i}_i(s) \end{bmatrix} = \begin{bmatrix} A_v(s) & Z_o(s) \\ Y_i(s) & A_i(s) \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix} \tag{20}$$

$Z_o(s)$ and $Y_i(s)$ are output impedance and input admittance respectively, generally used for the stability analysis of the cascaded system. $A_o(s)$ is audio-susceptibility parameter used for the estimation of input-output noise-transmission and

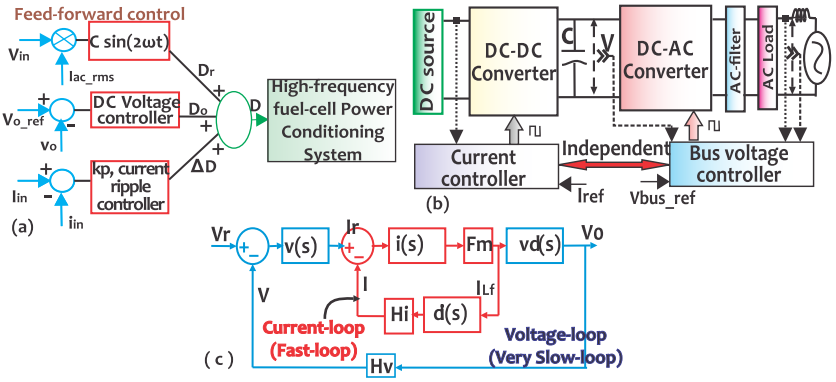

FIGURE 12. (a) Feed-forward scheme [34]. (b) Independent current & voltage loops [105]. (c) Dual loop control with very low voltage loop bandwidth [106].

TABLE 3. Comparison of simulation results for different voltage-loop bandwidths or f_v [107](see Fig. 14).

Parameters	$f_v = 2.4Hz$	$f_v = 30Hz$	$f_v = 65Hz$
1) % 2ω-ripple in input current	4.5	21	125
2) %Overshoot/ Undershoot in DC link voltage	+37/-29	+7.9/-10.5	+4.5/-4.7
3) Settling time (ms) of voltage at load application/removal	600/250	130/50	20/10

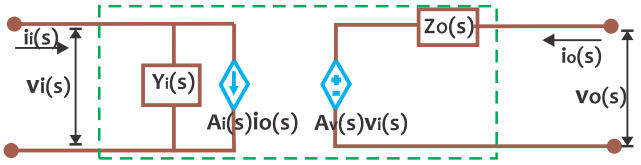

FIGURE 13. Two-port network of DC-DC converter: Hybrid parameters.

$A_i(s)$ is the back-current gain parameter. The parameters $Z_o(s)$ and $A_i(s)$ are used for the 2ω−ripple mitigation in the two-stage converters. However, $Z_o(s)$ parameter is widely explored in the output impedance shaping methods and a few methods have used $A_i(s)$ parameter (see Fig. 18) [108].

In the output-impedance shaping method, the control modifies the output-impedance of the front-end DC-DC converter such that the 2ω−ripple see more impedance in the direction of DC source. This method achieves the ripple-suppression at the input, however the control causes poor dynamic performance of system; the high output-impedance of system leads to poor system dynamics [109], [110]. In both the methods (i.e. dual-loop control method and output-impedance-shaping), there is a need to maintain the sufficient bandwidth of the voltage-loop throughout the desired frequency band of the operation.

Recently, some modified and improved control techniques have been proposed using the above mentioned concepts to minimize the 2ω−ripple at the DC input and to improve the system response simultaneously [17], [33], [58], [105], [108], [111]–[118]. These control schemes use resonant filters, for instance, notch-filter (NF) or band-pass filter (BPF) in the current or voltage loop. The basic principle is to minimize the 2ω-ripple in the reference of input current or to sufficiently reduce the bandwidth of the voltage-loop at 2ω only while maintaining high bandwidth of the voltage-loop at the other frequencies. The similar methods have been presented in the context of the power-factor correction (PFC) AC-DC converter [13], [14], [74], [119], [120]. However, the focus of this work is limited to review the existing literature in the context of the DC-AC power converter or inverter. The band-pass filter (BPF) and notch filter (NF) are generally used to mitigate the 2ω−ripple without affecting the dynamic performance of the system. The characteristics of BPF and NF are shown in the Fig. 15(a) and Fig. 15(b) using the Bode-plot. The BPF allows to pass a certain range of the frequencies of the input signal. The output signal leads the input signal by $\pi/2$ *rad* in 0 to ω_o range and lags by $\pi/2$ *rad* beyond the ω_o. Therefore, a total of π *rad* phase-shift occurs. The NF filter has inverse characteristics of the BPF. The NF allows all the frequencies except the frequencies located in a very narrow range of the resonance frequency (ω_o). A notch-filter also gives a phase-change of π *rad* for a transform of the input signal to the output signal, the phase is negative for the frequencies below ω_o.

In [16], the authors have proposed NF-added to the voltage-loop in the dual-loop control for a standalone DC-DC-AC converter. The reference inductor current is generated by passing the output of voltage controller through NF. Therefore, the method is named as notch-filter inserted current reference (NF-CR) scheme. The control block-diagram is shown in the Fig. 15(c). The NF attenuates 2ω-signal in reference of the inductor current. This minimizes the 2ω−ripple in input current. In [105], a control scheme is proposed for a grid-connected two-stage converter. A current controller is used with the first-stage and DC bus control is achieved by the grid-connected DC-AC converter. The method adopts a grid-side based 2ω-ripple compensation. A quasi-notch filter (quasi-NF) is added in the voltage-loop of the second-stage of the converter. The transfer function of quasi-NF is,

$$G_{NF}(s) = \frac{s^2 + \frac{\omega_o}{Q_z}s + \omega_o^2}{s^2 + \frac{\omega_o}{Q_p}s + \omega_o^2} \tag{21}$$

Here, Quality factor, Q is related as $|Q|_{dB} = |Q_p|_{dB} - |Q_z|_{dB}$. $|Q_z|_{dB}$ and $|Q_p|_{dB}$ are the quality factors of zero and pole respectively. The quasi-NF provides a much smaller voltage-loop gain than the current-loop gain at 2ω. This minimizes the 2ω−ripple at the input. This method retains the good dynamic performance of the system at all other frequency except the frequencies about and at 2ω. However, Q of the quasi-NF should be designed properly. Similar to [105], an another grid-side based 2ω-ripple compensation is adopted in [17]. The control scheme is shown in the Fig. 15(d). The control avoids the interaction of current-loop and voltage-loop at 2ω. However, the control design is involved to develop an LTI model from the time varying system model (see Fig. 15(d)); the two multiplications just before and after the current controller (CC) make model time varying. All three methods discussed above use notch filter. The use of the notch-filter may introduce a significant negative phase-shift to the frequencies lower than the characteristic frequency of notch filter [115]. This may introduce instability to the system.

In [115], Zhang *et al*. have proposed a voltage mode control (VMC) based band-pass filter incorporated into the inductor feedback path for a buck-derived two-stage converter (see Fig. 16(a-c)). The method is based on the output-impedance shaping. In Fig. 16(a), a virtual impedance ($Z_v(s)$) is added in series with the inductor. The concept is, to increase the impedance of inductor branch at 2ω frequency

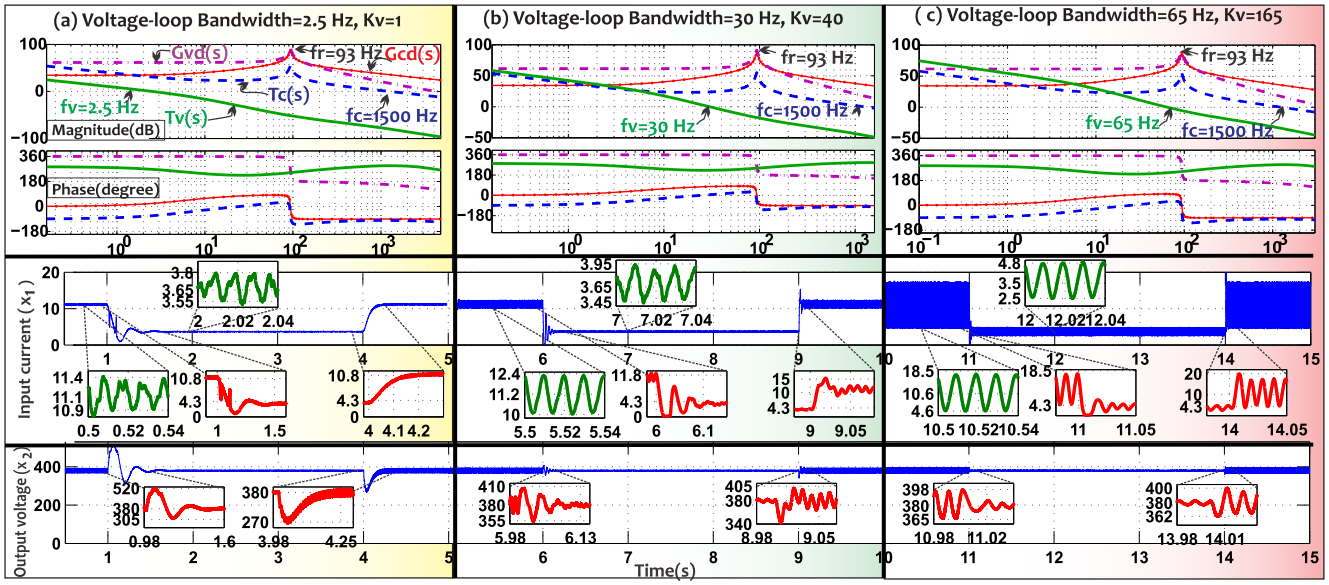

FIGURE 14. Effect of bandwidth of voltage-loop in dual-loop control: trade-off between ripple-reduction and dynamic performance of DC-DC-AC converter [107].

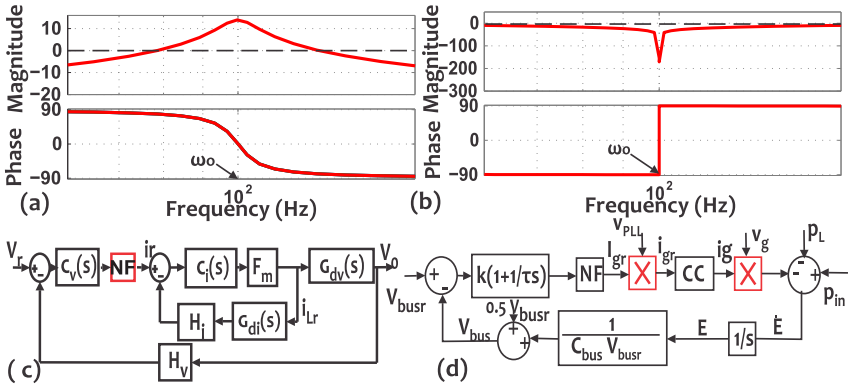

FIGURE 15. (a) Bode plot of BPF. (b) Bode plot of NF. (c) NF-CR control scheme [16]. (d) Control scheme based on NF proposed in [17].

such that the impedance of DC-link capacitor branch is less than the impedance of inductor branch. This compels the $2\omega-$ripple to pass through the capacitor instead of the inductor branch. Using Fig. 16(b), the impedance of the inductor branch is,

$$Z_o(s) = -\frac{v_c(s)}{i_L(s)} = \frac{sL + Z_v(s)}{1 + G_v(s)\frac{V_{in}}{V_m}H_v} \tag{22}$$

Here, G_v is voltage-loop controller, H_v is voltage sensor gain, V_m is PWM gain. $Z_v(s)$ is the virtual impedance added in the current feedback path. Suppose $Z_v(s)$ is a virtual resistance, *say* r_v. Therefore, the method can be named as virtual resistance scheme (VRS) [115]. In (22), an increase in $Z_o(s)$ is achieved by increasing the value of r_v. However, this decreases the magnitude of the loop-gain in the low frequency range [122]. To balance this, the gain of $Gv(s)$ can be decreased. However, this reduces the bandwidth of voltage-loop and hence degrades the dynamic performance of the system. Therefore, there is a trade-off between the design of r_v and bandwidth of the voltage-loop. Eventually, the results are the same as of the dual-loop control of [106]. This problem is solved by adding a BPF in the current feedback path instead of using a constant r_v only (see Fig. 16(c)). The BPF is tuned at 2ω and hence provides a high gain at 2ω only. This adds a high virtual impedance in series of inductor branch at 2ω. This reduces $2\omega-$ripple at the DC input without affecting the dynamic performance. However, adding a BPF leads a $-\pi/2$ to $\pi/2$ phase-rotation about the characteristic frequency of the BPF. Therefore, in [58], Zhang *et al*. further extended their work to resolve the challenges of [115] by adopting the current mode control (CMC) approach for the buck-derived two-stage converter. The work has presented different improved control strategies. The first control strategy, namely notch filter-inserted load current feed-forward scheme (NF-LCFFS), is realized by adding an NF in the load current in a feed-forward way

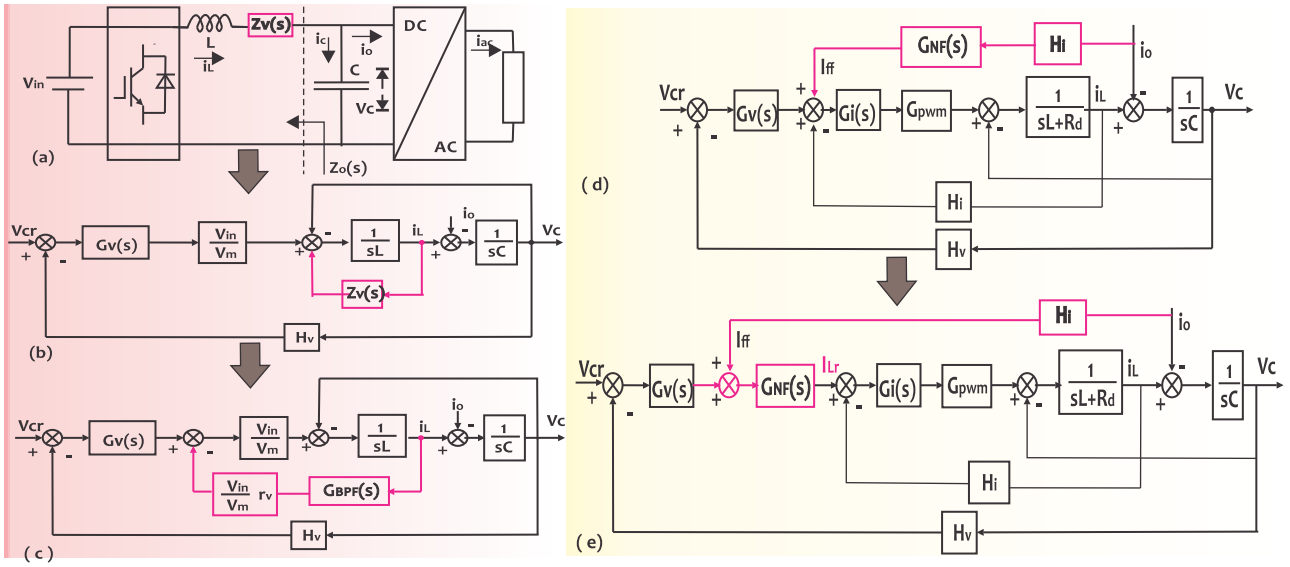

FIGURE 16. (a)-(b)-(c) A BPF based control scheme proposed in [115]. (d) NF-LCFFS and (e) NF-CR-LCFFS proposed in [58].

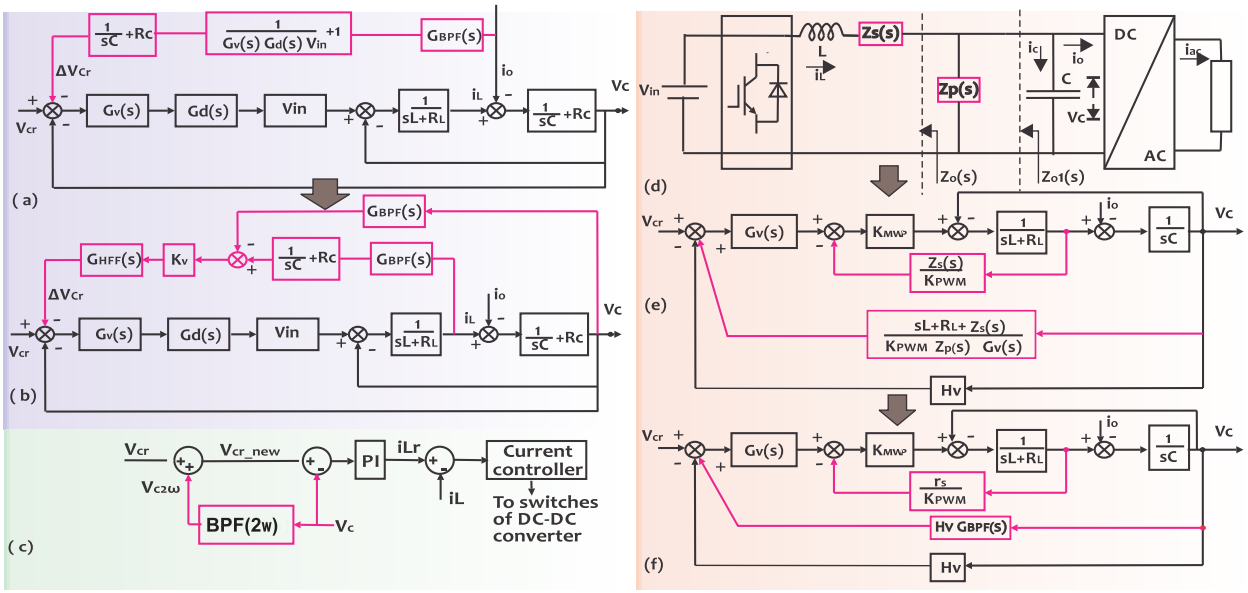

FIGURE 17. (a)-(b) VMC-LCFFS proposed in [121], (c) CMC-based control scheme proposed in [111], and (d)-(e)-(f) BPF-CVFS proposed in [33].

(see Fig. 16(d)). It is worth noting that the load current feed-forward control schemes improve the dynamic performance at the load-transients [123]. Therefore, the dynamic performance of the system is better. The NF attenuates the 2ω-ripple in the current-loop, therefore the $2\omega-$ripple reduces at the input of the two-stage converter. However, the voltage-loop in the Fig. 16(d) may contaminate the reference current of the inner-loop. Therefore, a further improvement is proposed by merging NF-CR scheme of [16] with the NF-LCFFS, and hence called NF-CR+LCFFS. It is worth to note that the NF-CR scheme has an NF already to minimize 2ω-ripple from the current reference of the inner-loop. A simplified block diagram is shown in the Fig. 16(e) where the two NFs are transformed to one. A single NF added at the output of the summing point after the voltage controller eliminates the requirement of the two NFs. This scheme almost eliminates the $2\omega-$ripple and also improves the dynamic performance of the system. However, the feed-forward schemes are susceptible to the disturbances and lack of the robustness as mentioned before. Moreover, NF may induce instability to the system as it affects the bandwidth of the voltage-loop. A detailed analysis and comparison of the control schemes of [115] and [58] are presented in [33]. A voltage control mode based load-current feed-forward scheme (VMC-LCFFS) is proposed in [121]. The control block-diagram of the VMC-LCFFS is shown in

the Fig. 17(a). The 2ω−ripple reduction utilizes the concept of modification in the reference value of DC-bus voltage in agreement with the desired pulsation in the DC bus voltage at 2ω. This makes DC-bus capacitor to have nearly all the 2ω−ripple. It is to be noted that the bus voltage is no longer constant but pulsates at 2ω (due to the addition of ΔV_{cr} term with V_r). A BPF is required with the load current feed-forward path to take-out the 2ω−ripple from the load current (i_o) which then generates a desired ΔV_{cr} that is to be added in V_r. The presence of integrator in the LCFFS path result into continuous integration action. This results into the rapid growth of the DC-bias in the LCFFS controller that leads to incorrect voltage tracking. Therefore, a high-pass filter (HPF) is also added at the end of LCFF path (see Fig. 17(b)). The scheme minimizes the 2ω−ripple while retaining the good dynamic performance. However, the control design is involved and the control of the VMC-LCFFS depends on the accuracy of the system parameters. A simple CMC-based control method for the said problem is proposed in [111]. This control scheme is similar to the control scheme proposed in [121]. The control block diagram is shown in the Fig. 17(c). The DC-link voltage reference is modified by adding $V_{c_{2\omega}}$. The $V_{c_{2\omega}}$ is extracted by passing the DC-link voltage through a BPF. The modified reference voltage $V_{cr_{new}}$ having 2ω voltage ripple cancels 2ω-voltage ripple of the actual DC-link voltage (v_c). This results in a ripple-free current reference in the current control-loop. A comparison of these control schemes is given in the [33] in the perspective of the output-impedance shaping. A similar control scheme i.e. BPF-incorporated capacitor voltage feedback scheme (BPF-CVFS) as presented in [111] is discussed in [33]. However, this control scheme is based on VMC method unlike the CMC method of [111]. The block-diagram of BPF-CVFS is shown in the Fig. 17(d-f). These all control schemes of [58], [115] are discussed for a buck-derived DC-DC-AC converter. These schemes are further explored for the boost converter in [117].

An effective use of the NF and BPF is proposed in [108] with the back-current gain based approach (using $A_i(s)$). The control block-diagrams are shown in the Fig. 18(a-b).

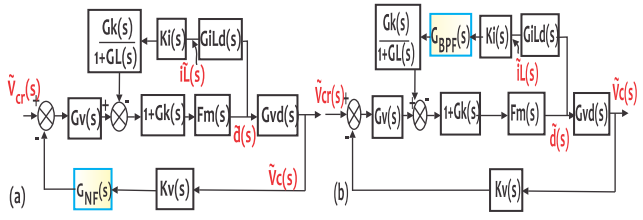

FIGURE 18. Back-current gain based scheme with (a) NF (b) BPF.

$A_i(s)$ relates input current ($i_{in}(s)$ with the output current ($i_o(s)$ of a system (e.g. DC-DC converter). In [108], it is established that for a VMC based control, the voltage-loop has a little effect on the 2ω-ripple attenuation. However, the 2ωripple reduction can be achieved for $\omega_o < 2\omega$. ω_o is the resonance frequency of LC circuit of the DC-DC converter. This is achieved by using average CMC scheme. However, this scheme also trade-off between ripple-reduction and dynamic performance. Therefore, further improvements in the back-current gain control scheme are made using (i) NF embedded in the voltage feedback branch and (ii) BPF embedded in the current feedback branch.

An 2ω−ripple mitigation technique is proposed in [124] for a fuel-cell sourced current-fed dual half bridge (CF-DHB) converter. A phase-shift control scheme is adopted that regulates the DC voltage and minimize the 2ω−ripple. The optimized duty is set to 0.5. The PI controls the DC-link voltage and a proportional resonant (PR) controller (tuned at 2ω) suppresses 2ω−ripple at the source. The PR controller modifies the main phase-shift angle to eliminates the input current ripple. The PR controller is similar to an integrator having infinite DC gain at characteristic frequency. Tuning PR to very low ω_o forces a difficult implementation of it on the low cost controller board (such as 16-bit DSP) [125]. In [126], authors have proposed a sinusoidal charging scheme for the dual-active-bridge based Si-charger and GaN-charger with the reduction in size of the capacitor at the DC-link using resonant controller and rotating frame control approach. The objective is achieved by injecting 2ω-ripple into the battery for the charging purpose. The size of DC-link capacitor decreases to 84% for Si-charger and 90% for GaN charger. However, this advantage comes after the ripple injection to the battery. The recent studies have addressed several detrimental effects of 2ω−ripple on the battery life [28]. Therefore, a long-term testing is needed for such schemes. In [118], Liu *et al*. have proposed a novel ripple compensator for a boost-derived-PV grid-connected inverter with battery-storage. The control scheme utilizes a double channel current feedback control to minimize the 2ω−ripple in the input current. The basic idea is to regulate the 2ω-voltage ripple in the DC-link voltage by adding a small disturbance of 2ω (*say* D_f) in the average duty (D_o). The Fig. 19(a) shows the control block-diagram. In the Fig. 19(a), G_f is a third-order general integrator (ToGI) filter (see Fig. 19(b)) to extract 2ω-component. A grid-side based bus voltage control is adopted. The voltage error of voltage-loop is passed through an NF. This eliminates the 2ω−component from the grid-side

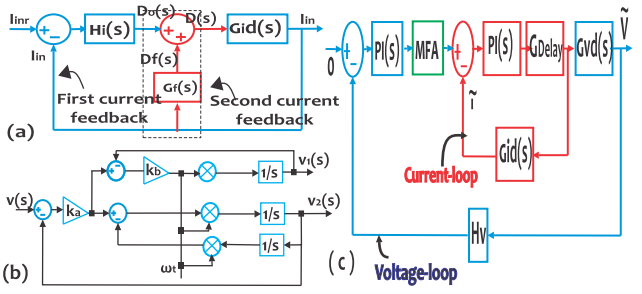

FIGURE 19. (a) Double input feedback and (b) third-order general integrator proposed in [118] (c) MAF based dual-loop control proposed in [127].

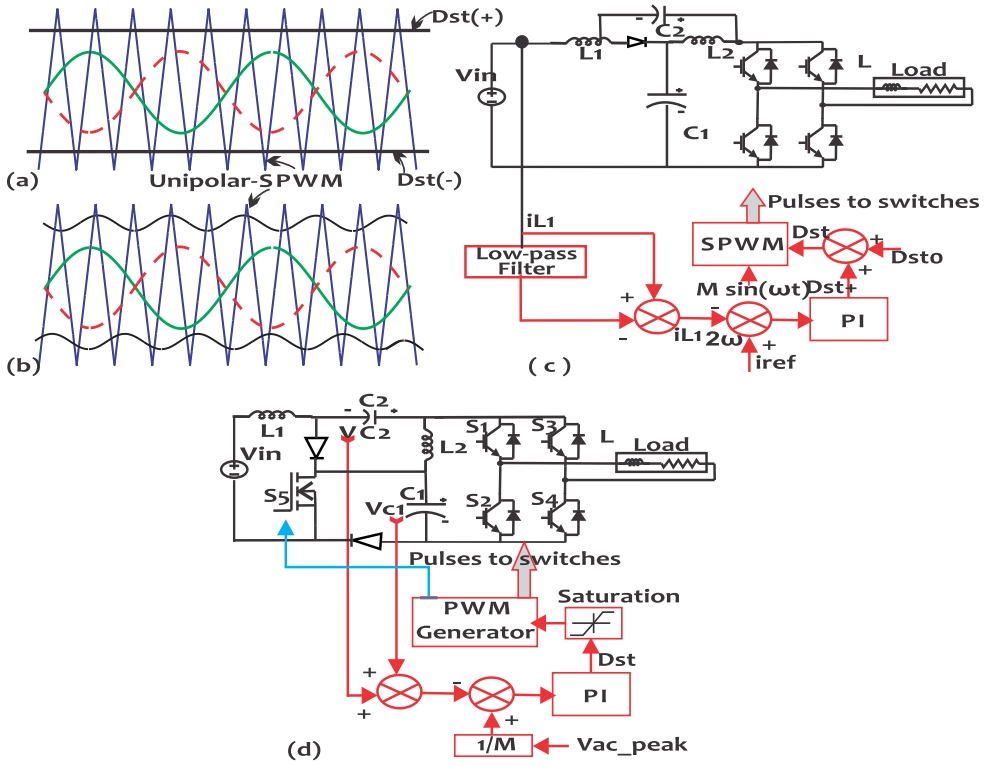

FIGURE 20. (a) Conventional shoot-through duty based-unipolar SPWM proposed (b) Modified shoot-through duty based-unipolar SPWM proposed in [64] (c) The low-pass filter based control scheme proposed in [62] (d) control scheme proposed in [101].

current reference. The current-error in the current-loop of the bus-voltage control is passed through proportional-resonant controller, this control the sinusoidal waveform of the grid current. A gain is multiplied with the output of G_f to regulate the value of $2\omega-$ripple. A large value of the gain minimizes the $2\omega-$ripple. However, this may induce instability to the system. Therefore, there is a trade-off between the stability and the ripple-reduction using a current feedback in the double-channel current feedback control. Use of multiple integrator in the $2\omega-$ripple-filter design may slow down the system dynamics. In [127], authors have proposed a dual-loop control for the boost-derived two-stage converter. The control scheme uses a moving average filter (MAF) in the voltage-loop to make the voltage-loop gain very low at 2ω. The control block diagram is shown in the Fig. 19(c). This scheme is similar to NF-CR of [16]. However, unlike NF-CR, this scheme can attenuates multiple of 2ω as well. In [112], another control scheme based on the MAF is proposed to control the swinging bus. The MAF has several advantages such as fastest step response, easy to implement using low-cost control-board, reduces random noise and notches the multiple of 2ω. However, the performance of MAF based on time-domain is better than the frequency-domain.

ZSI, quasi-ZSI, quasi-SBI eliminates the requirement of multiple stages. They can boost the input voltage and are capable of the shoot-through operation. In [64], authors have proposed a modified shoot-through duty based unipolar-SPWM technique as shown in the Fig. 20(b). The conventional technique is shown in the Fig. 20(a). The control forces the voltage across the capacitors of quasi-ZSI network to swing at 2ω or to store the all 2ω-decoupling power. This reduces the ripple at the DC input. However, in comparison to conventional method, the modified scheme introduces more voltage stress on the switches i.e. 53% more than conventional scheme. An optimum design of the quasi-ZSI network parameters is given in [62]. However, a part of the $2\omega-$ripple still flows through the quasi-ZSI network. The inductors store the decoupling power temporarily. It is better to transfer the stored decoupling power to capacitors; the power density of the capacitor is higher than inductor. Therefore, a PI regulator based control scheme is proposed in [62]; the control scheme is shown in the Fig. 20(c). The input current is passed through a low pass filter. This gives the DC current component which then subtracted from the actual input current to give $2\omega-$ripple. A PI controller generates the required pulsation in the equivalent shoot-through duty. The control scheme confines the ripple in capacitors and minimizes in the inductor current and input current. However, this method has a trade-off between stability and speed of response. In [101], a new quasi-SBI topology for the high voltage gain with a benefit of $2\omega-$ripple reduction is proposed. A thorough study is carried out to design the impedance network. A control scheme is added to keep the input ripple-free. The control method is shown in the

Fig. 20(d). The voltages of capacitors are added and then subtracted from the reference voltage. The DC-link voltage reference is generated based on the output voltage and modulation index. The voltage error is regulated to generate desired shoot-through duty. The application of this topology is limited to the low-power applications.

The non-linear control approaches are robust and suitable for system having large line-load transients. In [59], authors have proposed a dual-loop control method for the boost-derived-DC-DC-AC converter (see Fig. 21(a)). The ripple-reduction is achieved by adopting the output-impedance shaping. The control utilizes a sampled series feedback as the inner-loop. The series-feedback increases the output-impedance of front-end converter. A parallel feedback is added as outer-loop to regulate the DC-link voltage. However, the two feedback channels impose trade-off between the system dynamics and the ripple-reduction. Therefore, a non-linear compensator is added in between the voltage-error generation point and current controller. The non-linear compensator gives high gain at the load-transients to compensate the undershoot/overshoot in the DC-link voltage. However, an abrupt change in the gain may induce instability to the system. Therefore, a fine design of the non-linear compensator is required. A swing bus-voltage control is proposed in [128] for a stand-alone fuel-cell buck-derived two-stage converter. A nonlinear natural switching surface (NSS) based boundary control takes care of the very large input voltage-swing at 2ω. The controller minimizes the DC-link voltage swing and hence distortion in the output AC voltage. However, the practical implementation of such discontinuous variable frequency schemes based on the sliding mode control may introduce chattering effect in the switching [129]. In [130], [131], authors have proposed an adaptive switching function to minimize the 2$\omega-$ripple at the input of the boost-derived two-stage converter using the fixed-frequency based-SMC. The switching function is a combination of the inductor current error (e_1) and α times voltage error (e_2). α is power function of the e_2 i.e. $\alpha = \psi e_2^{\beta}$. β and ψ are design parameters. The profile of α is shown in the Fig. 21(b). For a very small value of α, the output-impedance is high, hence the ripple reduces at the input. At the line-load transients, α changes monotonically to converge the system dynamics at a faster rate. In [132], authors have proposed a SMC based

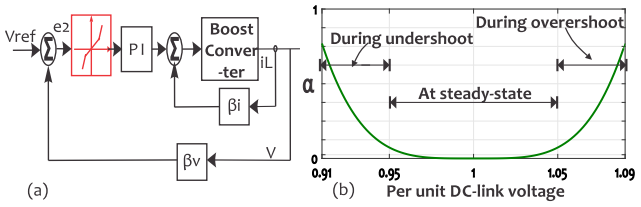

FIGURE 21. (a) Non-linear compensator technique proposed in [59] (b) Adaptive-SMC based ripple-mitigation technique proposed in [130].

phase cancellation technique for an $1-\phi$ grid-connected Quasi-Z-Source NPC Inverter. To cancel 2$\omega-$ripple the existing phase difference of π rad/s between capacitor voltage and inductor voltage at DC side is used.

It is to be noted that the control schemes presented in this Section still require a large size capacitor or an optimized value of the capacitance at the DC-link at the input-end of DC-AC converter [133]. The pulsation at DC-link are kept within the desired limit by choosing an optimum size of DC-link capacitor. Though the system performance at line-load transients is better despite the optimum size of DC-link capacitor which is achieved by different linear or nonlinear control approaches. To further minimize or eliminate 2ω-pulsation in the voltage at DC-link, an auxiliary circuit/active filter is added. In the next subsection, two-stage DC-DC-AC converter with the additional active filter are discussed.

2) CONTROL-ORIENTED COMPENSATION TECHNIQUES WITH ADDITIONAL ACTIVE FILTER

In [82], an active filter circuit connected at DC bus as shown in the Fig. 22(a) is proposed for the boost-derived two-stage converter. This filter is similar to the filter proposed in [69]. An SMC based nonlinear control techniques is used in [82]. The sliding mode controller regulates the active filter such that the filter injects a suitable compensation current in the DC-bus to cancel the effect of the 2ω-ripple. The compensation current is generated using ADLINE neural filter. However, the design of the neural filter is a challenge. The voltage of the C_b in the Fig. 22(a) should kept higher than the DC-bus voltage. Therefore, the system has a higher voltage than DC-link that causes the safety concern. A block diagram of the 360 W-Texas Instruments UCC28180EVM-573 front-end evaluation board integrated with the buck-boost type bidirectional active filter is shown in the Fig. 22(b) [134], [135]. To control the active filter, a multi-resonant direct voltage regulation technique is used to decouple the 2ω-power ripple at the DC-link. The control scheme makes the active filter to mimic an infinite capacitance parallel to the DC-link. The active filter is controlled using a modified dual-loop control scheme as shown in the Fig. 22(c). The parallel resonant filters tuned at the multiple of 2ω are added in the voltage-loop. The filters attenuate multiple of 2ω components from the reference current of inner-loop. The multi-resonant resonant filters are similar to MAF used in [19]. At the load-transients, the voltages across the DC-link capacitor and active filter side capacitor show abnormal behavior and hence the load-transient behavior of the system is a challenge. For the circuit of active filter (buck/boost/buck-boost type) shown in the Fig. 22(d), an one-cycle control method has been proposed in [133]. The switches of active filter are controlled such that per cycle average value of the current at the output of the active filter tracks 2ω-current ripple at the DC-link. The control utilizes the peak-value of ripple storage capacitor, therefore a peak detector is required to realize the peak voltage control. An application of buck-boost type APT along with zero voltage switching is proposed in [138] to reduce the switching loss also. A bidirectional

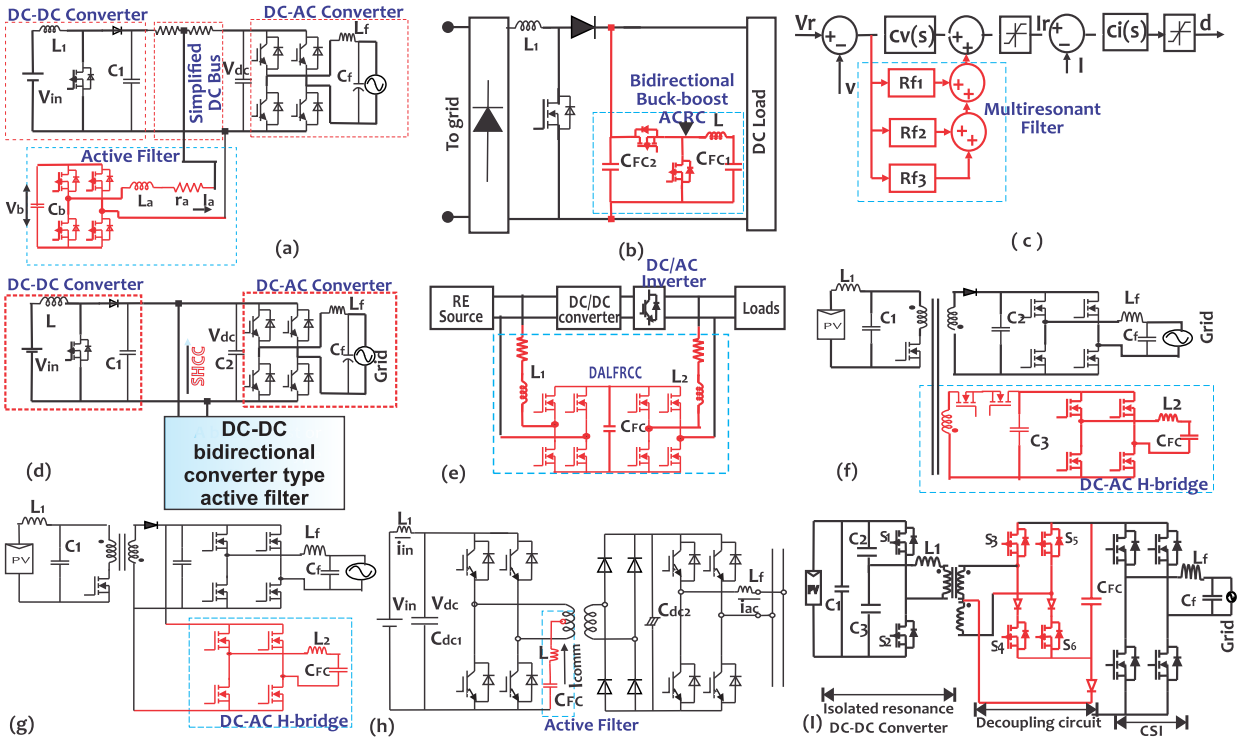

FIGURE 22. (a) Active filter proposed in [82] (b) active filter proposed in [134], [135] (c) control scheme for active filter proposed in [135] (d) active filter proposed in [133] (e) DALFRCC [136] (f) integrated H-bridge active filter and (g) auxiliary winding based H-bridge active filter proposed in [83] (h) Common-mode operation based technique for half-active bridge proposed in [98] (i) DC to single-phase AC grid-connected converter [137].

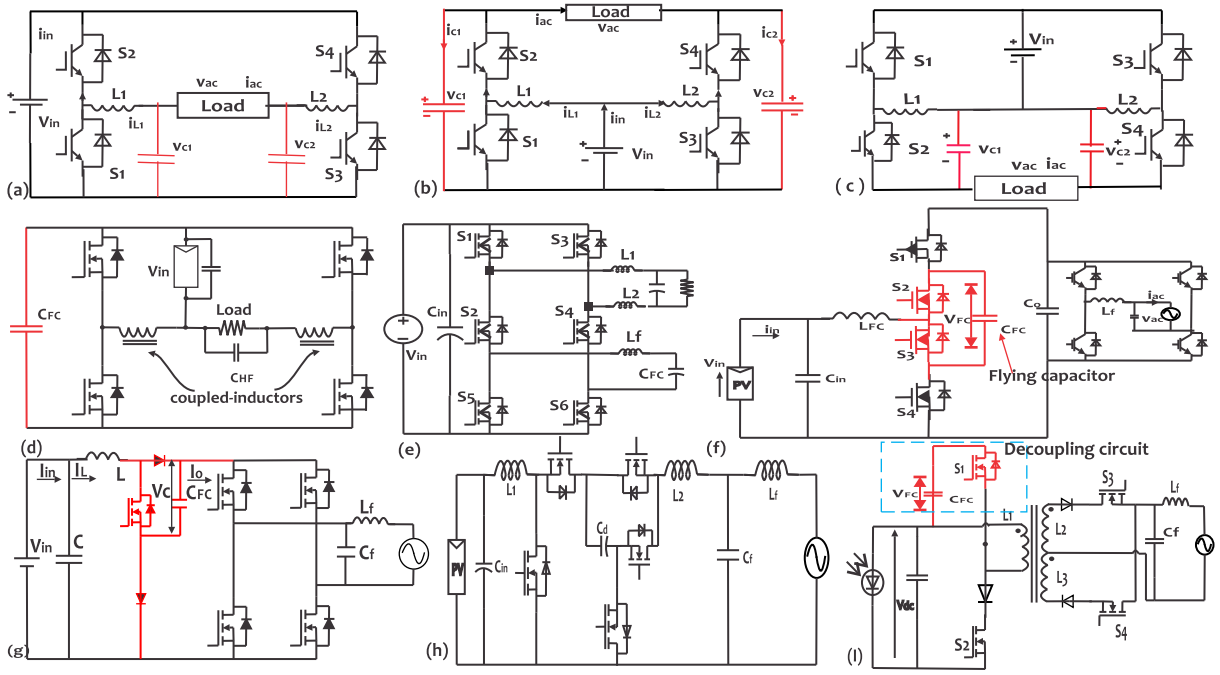

FIGURE 23. Some other topologies and ripple mitigation techniques:(a) Buck-type differential inverter (b) Boost-type differential inverter (c) Buck-Boost-type differential inverters (Fig. 23(a-c) [90], [139]–[141])(d) Coupled-inductor based PV inverter [142] (e) Six-switch topology [143] (f) Flying capacitor based topology [81], [144] (g) Modified-boost-derived two-stage converter [145] (h) Cuk converter based five-switch single-phase inverter [146] (i) Flyback type single-phase utility interactive inverter [147].

dual-active low frequency ripple control circuit (DALFRCC) shown in the Fig. 22(e) can alleviate the ripple from the input and a 90% compensation of $2\omega-$ voltage ripple at DC-bus can be achieved [136]. However, the active filter has eight switches. This makes the system costly and complex. Additionally, two linear neural filters are used to

generate the compensation current commands corresponding to i_a and i_b (see in Fig. 22(e)). A sliding mode controller is proposed for the injection of compensation currents at DC bus and AC output terminal. However, design of the neural filters is complex and a challenge. The integrated and auxiliary winding based inverter topologies as shown in the Fig. 22(f) and Fig. 22(g) respectively are proposed in [83]. The active filter or ripple-port are the H-bridge inverter. The control scheme is based on the power ripple balancing given by (9)-(14). The active filter eliminates the large E-cap. However, the number of switching devices is increased. In [98], an economical active filter with no extra switching devices is proposed for an isolated half-active bridge two-stage DC-DC-AC converter. In the Fig. 22(h), the main circuit with active filter is shown. An LC filter circuit is connected between the center-taping connection point of the primary winding of the transformer and the return wire of the active-bridge at primary. The control scheme of LC filter is based on the common mode operation method. The control scheme reduces the size of the capacitor at the DC link and also the switching devices are the same as used in the conventional system. However, the rating of the switching devices is increased due to the flow of the active filter current in the transformer and the first-stage of the converter. The control of the active filter limits the transformation ratio of the transformer. Fig. 22(i) shows a circuit of a resonance type DC-DC converter, power decoupling circuit and current source inverter (CSI). The control scheme achieves a power decoupling by controlling the charging and discharging of the buffer capacitor (C_{FC}) such that the input power is equal to the output power. Therefore, the input is ripple-free while C_{FC} takes all the pulsation. The resonance type DC-DC converter makes a series resonance circuit. The quality factor of this circuit should be kept very high in order to ensure stability. To improve the efficiency of the system, the size of the inductor in the resonating circuit should be decreased.

D. SOME OTHER TOPOLOGIES AND TECHNIQUES

In Fig. 23(a-c), the buck, boost and buck-boost differential inverter (DI) topologies are shown respectively [90], [139], [140]. In [148], a generalized power decoupling method is proposed for DI with the non-linear load. The proposed control techniques is similar to the control technique proposed in [135]. According to analysis presented in [148], the buck-type DI has lowest switch voltage stress and small decoupling capacitor. However, the DC-link voltage should be kept high. The boost-type DI requires low DC-link voltage. However, the voltage stress on the capacitors and current stress on the switches are high. The buck-boost type DI achieves the lowest DC-link voltage requirement and it can compensate the most of the harmonics. However, this topology suffers the highest switch-voltage stress. In [90], authors have proposed a waveform-control (WFC) method [149] based ripple-mitigation for a boost-type DI [141] as shown in the Fig. 23(b). A brief of the WFC is as follows [90].

In the Fig. 23(b), the voltage across the AC load is given by the sum of the voltages across the capacitors v_{c1} and v_{c2}. The two voltages are out of the phase. This implies,

$$v_{c1} = V_{off} + 0.5V_m sin(\omega t) \tag{23a}$$
$$v_{c2} = V_{off} + 0.5V_m sin(\omega t - \pi) \tag{23b}$$

Here, V_{off} is offset-voltage of capacitors. V_m is maximum value of output AC voltage (v_{ac}) and ω is angular frequency of AC power supply. The instantaneous output AC voltage is,

$$v_{ac} = v_{c1} - v_{c2} = V_m sin(\omega t) \tag{24}$$

Basic idea of ripple-reduction is to reshape the waveform of voltages across the capacitors without affecting output AC voltage. For this, a function $x(t)$ is added in (23b) as follows,

$$v_{c1} = V_{off} + 0.5V_m sin(\omega t) + x(t) \tag{25a}$$
$$v_{c2} = V_{off} + 0.5V_m sin(\omega t - \pi) + x(t) \tag{25b}$$

Suppose $x(t) = Xsin(2\omega t + \phi)$ with amplitude X and a phase ϕ with respect to the reference. For $C_1 = C_2 = C$, the current through the capacitors are,

$$i_{c1} = 0.5\omega CV_m cos(\omega t) + 2\omega CXcos(2\omega t + \phi) \tag{26a}$$
$$i_{c2} = -0.5\omega CV_m cos(\omega t) + 2\omega CXcos(2\omega t + \phi) \tag{26b}$$

In the Fig. 23(b), the input current (i_{in}) is,

$$i_{in} = i_{L1} + i_{L2} \tag{27}$$

Here, $i_{L1} = \frac{i_{ac}+i_{c1}}{1-D_1} = \frac{(i_{ac}+i_{c1})v_{c1}}{v_{in}}$ and $i_{L2} = \frac{i_{ac}+i_{c2}}{1-D_2} = \frac{(i_{ac}+i_{c2})v_{c2}}{v_{in}}$, where $i_{ac} = I_m sin(\omega t)$ and D_1 and D_2 are the duty cycles of the switches S_1 and S_3 respectively. Using these in (27) gives,

$$i_{in} = \frac{\begin{bmatrix} V_m I_m + 2\omega X^2 Csin(4\omega t + \phi) - V_m I_m cos(2\omega t) \\ +0.5\omega CV_m^2 sin(2\omega t) + 8\omega XCV_{off} cos(2\omega t + \phi) \end{bmatrix}}{2V_{in}} \tag{28}$$

Clearly, to eliminate 2ω-ripple from the input current, 2ω-component of (28) should be zero. This gives,

$$X = \frac{V_m\sqrt{I_m^2 + (0.5\omega V_m C)^2}}{8\omega V_{off} C} \tag{29a}$$
$$\phi = 0.5\pi - sin^{-1}\frac{I_m}{\sqrt{I_m^2 + (0.5\omega V_m C)^2}} \tag{29b}$$

The waveform control method eliminates requirement of additional active filter. However, the performance of WFC may be affected by the tolerance of capacitors and inductors of DI [150]. An improved version of the WFC is proposed in [150] applying a rule based control (RBC) method on the WFC. In the RBC, the values of X and ϕ are perturbed accordingly to achieve ripple mitigation despite the variations in system parameters. However, in the RBC, a large perturbation may lead to the poor performance of ripple-reduction and very small perturbation may affect the dynamic performance

of the system. To get rid-off dependence of WFC on the system components, authors of [150] further proposed an input current feedback control method in [151]. In [142], a coupled-inductor based PV inverter with an advantage of the power decoupling is proposed. The circuit of this topology is shown in the Fig. 23(d). An input voltage high bandwidth controller is proposed for this circuit to keep 2ω-ripple in the capacitor (C_{FC}). In this topology, the common-mode leakage is a problem due to its transformer-less configuration. In [143], a six-switch topology is proposed (see Fig. 23(e)). This topology has a combined feature of the inverter and rectifier. The switch S_2 is shared by rectifier and inverter both. The phase difference of modulation references are varied to achieve 2ω-ripple reduction at the DC link. However, in this topology, the phase difference is constrained by the input and output unlike the conventional topology where the phase difference can be kept between $-\pi$ *rad* to $+\pi$ *rad*. A modified version of the conventional front-end DC-DC boost converter in a two-stage converter is proposed in [81], [144]. This topology uses flying capacitor in place of the large size electrolytic capacitor (see Fig. 23(f)). This capacitor is used for voltage boosting and 2ω-power-decoupling. The control scheme forces the voltage of the flying capacitor to fluctuate at 2ω to decouple the ripple instead of the DC-link voltage. An another modified version of the boost-derived two-stage converter is proposed in [145] (see Fig. 23(g)). There are four switching modes of the operation. In the first and fourth modes, the modified boost-circuit functions like the conventional boost converter. In the second mode, the buffer capacitor is charged with the required decoupling energy and in the third mode, the stored energy is supplied to the inverter-load. Therefore, the DC-link capacitor is not required to supply the 2ω-ripple power. This makes the DC-link ripple-free. In [146], authors have proposed a Cuk converter based five-switch single-phase inverter topology (see (see Fig. 23(h)) for 2ω-ripple-mitigation. The interaction between input and output is avoided using a switching sequence to decouple the ripple at the input. A flyback type single-phase utility interactive inverter with the power-decoupling capability is proposed in [147]. The control achieves the ripple-free input current by storing the decoupling power in the capacitor, C_{FC} of the circuit in Fig. 23(i). The proposed topology is simple, cost-effective and small in the size.

IV. CONCLUSIVE DISCUSSION AND CHALLENGES

This paper has reviewed several passive and active power decoupling techniques, and its subcategory nominated as control-oriented compensation techniques for the single-phase inverters. The work is summarized in Table 4-5.

The Passive power decoupling techniques (PPTs) utilizes passive components (L,C) for the power decoupling. Use of E-cap is the simple and conventional technique. Other than the cost, size and weight of E-cap; the reliability of E-cap is a major concern. Even though the film-capacitor minimizes reliability problem, it adds the cost, weight and size to the system. The use of film capacitor with the power-electronics circuit as the active filter gives one of the best possible solutions to eliminate E-cap. A comparatively small size film capacitor is used in the active power decoupling techniques (APTs). The APTs can be applied to the DC-side and AC-side (mixed-type) applications. The DC-side application of APTs is easy and does not affect the H-bridge circuit. However, the control scheme should be designed accordingly. The basic control approach is, to balance the decoupling power at the DC-link by the power exchange with the film capacitor. The AC side APT is comparatively better on the basis of the efficiency of system due to its application at the AC side itself. However, the application of these techniques interfere the main H-bridge circuit. This modifies the modulation index of the inverter. This may lead to under-utilization of the power-electronics devices and increased stress on the components. The control is also a challenge. In both DC side and AC-side applications of the APTs, the number of the components increases. This reduces the over-all efficiency of the system and increases the size, cost and complexity of the control method.

The two-stage DC-DC-AC converters and the single-stage converters with front-end control-capability have inbuilt option of the active control. The front-end DC-DC converter can be utilized for the input $2\omega-$ripple-mitigation purpose. The software based control-oriented compensation techniques (CCTs) are generally utilized in such systems. The dual-loop control scheme and output-impedance shaping scheme are two popular CCTs. The former scheme aims to minimize the $2\omega-$ripple in the reference current of inner-loop in order to compensate $2\omega-$ripple in the input current by significantly reducing the bandwidth of voltage-loop. The later scheme aims to increase the output impedance of the front-end converter such that $2\omega-$ripple is forced to flow through the DC-link capacitor branch. However, both the schemes suffer the poor dynamic performance. The addition of resonant filter in the current or voltage loop has shown improved dynamic performance. The addition of notch-filter with resonance frequency at 2ω in voltage-loop in the dual-loop mode control scheme provides enough separation between voltage-loop and current loop and hence 2ω-ripple reduces at the input of the system. This scheme improves dynamic performance of the system, however, this limits the bandwidth of system for a wide-range frequency operation due to the addition of negative phase-shift by the notch-filter for the frequencies below the resonance frequency. A poor-design of the resonant filter may induce instability. In case of voltage mode control scheme, an addition of band-pass filter with the resonance frequency at 2ω is used to increase the output-impedance of the front-end converter to achieve the mitigation of 2ω-ripple. A good dynamic performance of the system is achieved with this scheme, however, a phase rotation of π rad/s by the band-pass-filter limits voltage-bandwidth of the system.

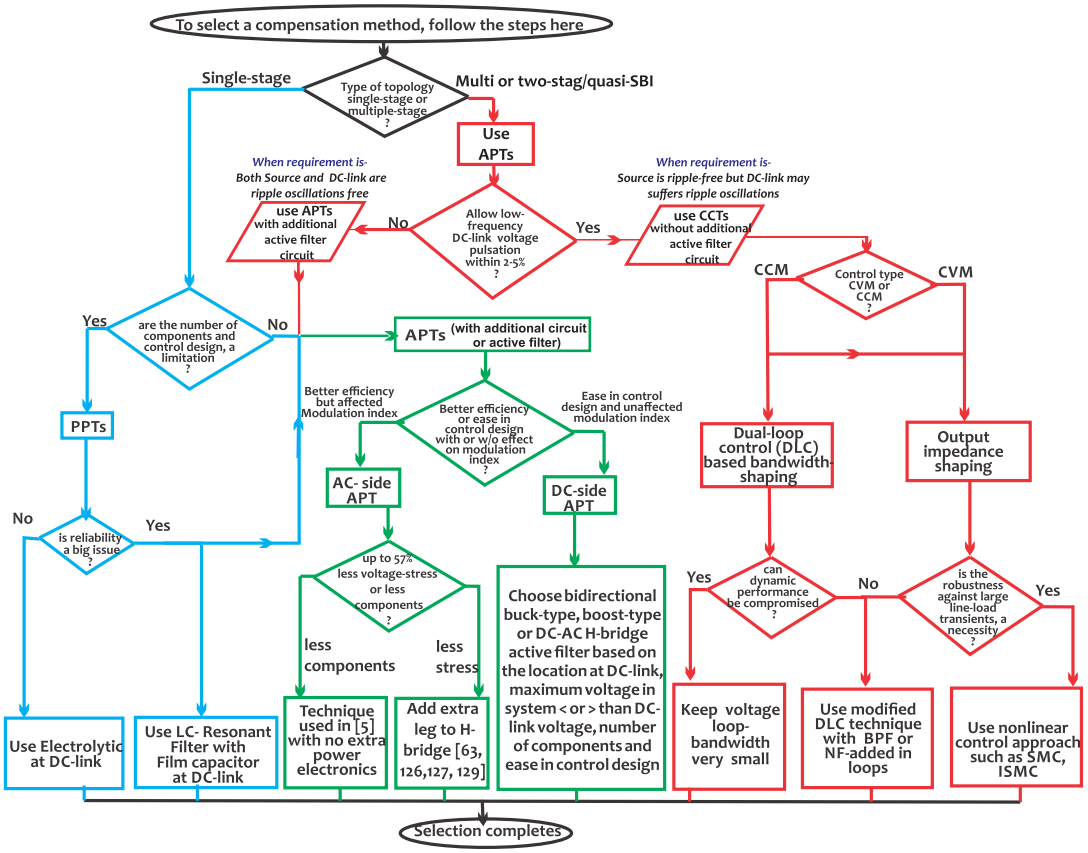

FIGURE 24. Algorithm for the selection of suitable 2ω−ripple compensation technique in a broader sense.

TABLE 4. Summery of passive and active techniques.

Ref./Fig.	Technique	Extra Components	Scheme or tool	Merits	Challenges
[1]/Fig. 9(a)	APT (AC-side)	2-C	Passive components	No extra switches addition	Efficiency affected, utilization factor of storage elements$<50\%$
[19]/Fig. 6(f)	APT (DC-side)	4-S,1-L,1-C	Ripple-port Circuit	Better system life	More switches
[67]/Fig. 6(d)	APT (DC-side)	2-S, 1-L, 1-C	Buck-type filter (bidirectional)	No voltages $> V_{DC-link}$ in the system	DCM operation causes high current stress
[36]–[41]/Fig. 5	PPT	A large size E-cap	E-cap	Simple and conventional technique	Reliability issue, high, ESR value low-ripple handling capacity
[45], [56]/Fig. 5(f)	PPT	1-L,1-C	Inductive filter	Easy and smaller	Large size inductor
[57]/Fig. 9(g)	APT (DC-side)	6-S, 2-C, 1-L, 1-Txr	Hybrid filter	Small size buffer capacitor	More components and lossy
[63]/Fig. 10	APT (AC-side)	2-S, 1-C, 1-L	Integrated filter	Small capacitors in qZSI	One extra leg
[152]/Fig. 5(k)	PPT		LC-resonant filter	Cost-effective with LC	resonance problem, tedious L-C design
[66]/Fig. 6(b)	APT (DC-side)	2-S, 1-C, 1-L	ALFRCD	Small filter size	Possibility of short-circuiting for $v_{FC} < v_{DC-link}$
[65]/Fig. 9(f)	APT (AC-type)	2-S, 2-C, 1-L 1-Txr, 1-Rcr	CPS-PAF Buck/Boost type	Possible problem of short-circuiting solved	LFT and a rectifier required, Bulky and complex system
[69]/Fig. 6(e)	APT (DC-side)	4-S, 1-L, 1-C	FB-RCR	LFT and rectifier not required	4-switches are required
[86]/Fig. 8(b)	APT (DC-side)	2-S, 1-C, 1-L	Buck-boost type filter for qZSI	Smaller size of Z-source network	Challenging control design compared to H-bridge
[87]/Fig. 8(c)	APT (DC-side)	Battery	quasi-ZS network with battery	Detailed design of asymmetric quasi-ZS network is available	A part of 2ω−ripple can be reduced
[88]/Fig. 8(d)	APT (DC-side)	2-S, 1-C, 1-L	Boost type APT	Complete ripple decoupling	Design of PR controller
[91]/Fig. 9(b)	APT (AC-side)	2-S	Ripple-confinement	100% utilization of storage elements	One extra leg besides H-bridge more voltage stress on switches
[92]/Fig. 9(c)	APT (AC-side)	2-S, 1-C, 1-L, 2-E-cap	SVPWM Based	Current and voltage stress is less for a range of power-factor	One extra leg device power rating besides H-bridge, total increase by 50%
[93]/Fig. 9(d)	APT (AC-side)	2-S, 1-C, 2-L	Active filter	Stress on switches reduces by 70% for all power factor ($p.f.$)	One extra leg besides H-bridge
[94]/Fig. 9(e)	APT (AC-side)	2-S, 1-C, 1-L	Active filter	Switch-stress reduces by 70% for all $p.f.$	High cost of GaN switches
S=Switch	C=capacitor	L=inductor	Txr=Transformer	Rcr=Rectifier	

The nonlinear control approaches are generally preferred in the system with the large line-load disturbances such as RE sources based power systems. Furthermore, the RE sources are sensitive to low-frequency ripple. Therefore, the non-linear control approaches are suitable in such applications. The nonlinear control approaches perform well at the large line-load transients in comparison to the linear controllers. The nonlinear controls such as SMC and ISMC add high degree of robustness against the matched uncertainty. Nevertheless, in the literature, a few nonlinear control techniques are proposed for the mitigation of the $2\omega-$ripple problem. The added features of the robustness and the stable wide range of operation at the large line-load transients over the linear controls, the nonlinear control approaches are to be explored thoroughly in the context of the mitigation of $2\omega-$ripple problem in the single-phase inverter.

Z-source inverters (ZSIs) and quasi-ZSIs are the emerging competitive technologies for medium/high power applications. Similarly, the switched-mode boost inverters and quasi-switched boost inverters are emerging technology in the low-power applications especially for microinverter

TABLE 5. Summery of control-oriented compensation techniques in DC-AC converters with front-end converter or control circuits.

Ref./Fig.	Topology	Scheme or tool	Basic concept	Remarks
[16]/Fig. 15(c)	Two-stage; stand-alone; Push-pull forward type DC-DC-AC converter	NF-added; voltage-loop(CMC)	NF attenuates 2ω-ripple in reference current of current-loop	NF adds negative phase for frequencies$< \omega_o$ may cause instability
[17]/Fig. 15(d)	Two-stage;Grid-connected; isolated-phase-shift DC-DC-AC converter	NF-added voltage-loop, grid-side bus voltage control	similar to [16]	Same as in [16] complex control design
[33]/Fig. 17(d-f)	Two-stage; buck-derived DC-DC-AC converter	BPF-CVFS (CVM)	2ω variation in reference bus voltage	same as in [115]
[34]/Fig. 12(a)	Two-stage;Grid-connected Current-fed resonant push-pull DC-DC-AC converter	Feed-forward control	Feed-forward generates ripple cancellation duty	Easy to implement, poor disturbance-rejection, lacks robustness
[58]/Fig. 16(e)	Two-stage; stand-alone Buck-derived DC-DC-AC converter	NF-LCFFS (CMC)	NF in load current feed-forward path decreases Z_o everywhere except at 2ω	NF adds negative phase for frequencies$< \omega_o$
[58]/Fig. 16(e)	Two-stage; stand-alone; buck-derived DC-DC-AC converter	NF-CR-LCFFS (CMC)	NF-CR-LCFFS decreases Z_o everywhere except at 2ω	NF adds negative phase shift, limited bandwidth
[59]/Fig. 21(a)	Stand-alone;Boost-derived DC-DC-AC converter	PI+Non-linear compensator	Output-impedance shaping	Instability problem due to high controller gain
[118]/Fig. 19(b)	Residential PV and Battery system	Double channel current feedback control, ToGI	Ripple-free duty control based	Trade-off b/w ripple-reduction and stability
[127]/Fig. 19(c)	Boost;buck-boost derived power converters	MAF or multi-resonant filter	Notching effect at multiple of 2ω	Attenuates 2ω-ripple and its multiple; a negative phase-shift occurs due to NF
[105]/Fig. 12(b)	Two-stage; Grid-connected Boost-derived converter	quasi-NF-added voltage-loop (grid-side control)	Notch-filter substantially reduces voltage-loop BW	quasi-NF adds negative phase for frequencies$< \omega_o$
[105]/Fig. 12(b)	Two-stage; Grid-connected Boost-derived DC-DC-AC converter	Independent current loop & voltage-loop	No interaction between loops	Theoretically; a large reduction in 2ω-ripple; difficult implementation
[106]/Fig. 12(c)	Two-stage; stand-alone; DC-DC-AC converter	Dual-loop control(CMC)	Very low bandwidth (BW) of voltage-loop	Trade-off b/w ripple-reduction and dynamic performance
[108]/Fig. 18(a-b)	Half-active bridge DC-DC-AC converter	Back-current gain based control	Very small back-current gain at 2ω or minimum approach	NF adds negative phase; BPF causes $\pi\ rad$ phase rotation; limited BW
[111]/Fig. 17(c)	Current-fed push-pull based DC-DC-AC converter	similar to [121] (CMC)	2ω-variation in reference bus voltage to generate ripple-free current reference	Bandwidth limitation
[115] /Fig. 16(a)	Two-stage; Buck-stand-alone derived DC-DC-AC converter	VRS	A virtual resistance increases Z_o	poor dynamic performance
[115]/Fig. 16(c)	Two-stage;stand-alone Buck-derived DC-DC-AC converter	NF-CR; (CVM)	BPF in current feedback path increases Z_o at 2ω	a phase rotation of $\pi\ rad$ caused by BPF limits voltage-loop bandwidth
[121]/Fig. 17(a-b)	Two-stage; stand-alone Buck-derived DC-DC-AC converter	LCFFS (VMC)	Pulsation in DC-link voltage forces the ripple to follow capacitor branch	DC-link pulsates at 2ω; performance depends on system parameter's accuracy
[124]	CF-DHB DC-DC-AC converter	Phase-shift control; PR controller	PR modifies the main phase-shift control	PR limits the BW; sluggish dynamics
[126]	Dual-active bridge based GaN and Si-charger	Low-pass filter based control	sinusoidal charging forces ripple injection into battery	battery life may be affected
[128]	Stand-alone; fuel-cell based DC-DC-AC converter	NSS	four quadrant control	may suffer chattering problem
[130]/Fig. 21(b)	Stand-alone;Boost-derived DC-DC-AC converter	adaptive-SMC	Output-impedance shaping	Ripple-reduction affected during transients

applications. Unlike the two-stage converters, these all topologies constitute a single-stage units and have the capability of shoot-through operation. The reduction in the size of components of front-end networks of such converters, for instance, Z source or quasi-Z source network in the presence of 2ω-ripple is a challenge. Nonetheless, quasi-ZSI and quasi-SBI have inbuilt front-end control capability, and therefore ripple mitigation at the input can be achieved through the suitable control only without adding additional active filter.

To summarize, the reliability of E-cap, control and compact design of active filter, stability, dynamic performance and robustness of system against the uncertain characteristics of the RE/alternative energy sources based systems are open challenges. A flowchart, shown in the Fig. 24, is proposed here to conclude the literature reviewed in this paper.

REFERENCES

[1] I. Serban, "Power decoupling method for single-phase H-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4805–4813, Aug. 2015.

[2] Z. Wang, B. Wu, D. Xu, M. Cheng, and L. Xu, "DC-link current ripple mitigation for current-source grid-connected converters under unbalanced grid conditions," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4967–4977, Aug. 2016.

[3] N. Rathore, D. Fulwani, A. K. Rathore, and A. R. Gautam, "Adaptive sliding mode based loss-free resistor for power-factor correction application," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4332–4343, Jul. 2019.

[4] P. S. Almeida, V. C. Bender, H. A. C. Braga, M. A. D. Costa, T. B. Marchesan, and J. M. Alonso, "Static and dynamic photoelectrothermal modeling of LED lamps including low-frequency current ripple effects," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3841–3851, Jul. 2015.

[5] J. L. Stevens, J. S. Shaffer, and J. T. Vandenham, "The service life of large aluminum electrolytic capacitors: Effects of construction and application," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1441–1446, Sep. 2002.

[6] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Oct. 2014.

[7] E. D. Dunlop, D. Halton, and H. A. Ossenbrink, "20 years of life and more: Where is the end of life of a PV module?" in *Proc. Conf. Rec. 31st IEEE Photovoltaic Specialists Conf.*, Jan. 2005, pp. 1593–1596.

[8] G. Petrone, G. Spagnuolo, R. Teodorescu, M. Veerachary, and M. Vitelli, "Reliability issues in photovoltaic power processing systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2569–2580, Jul. 2008.

[9] E. Wolfgang, U. Drofenik, and W. Gerling, "Reliability of power electronic systems," ECPE Tutorial, Nuremberg, Germany, Tech. Rep., Apr. 2007.

[10] M. Bramoulle, "Electrolytic or film capacitors?" in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 33rd IAS Annu. Meeting*, vol. 2, Oct. 1998, pp. 1138–1141.

[11] Q.-C. Zhong, W.-L. Ming, W. Sheng, and Y. Zhao, "Beijing converters: Bridge converters with a capacitor added to reduce leakage currents, DC-bus voltage ripples, and total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 325–335, Jan. 2017.

[12] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[13] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[14] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de Rossiter Correa, "Low-frequency power decoupling in single-phase applications: A comprehensive overview," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2892–2912, Apr. 2017.

[15] B. Ge, X. Li, H. Zhang, Y. Liu, R. S. Balog, H. Abu-Rub, and L. Alpuerto, "Direct instantaneous ripple power predictive control for active ripple decoupling of single-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3165–3175, Apr. 2018.

[16] Z. Wei, X. Deng, C. Gong, J. Chen, and F. Zhang, "A novel technique of low frequency input current ripple reduction in two-stage DC-AC inverter," in *Proc. IECON 38th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2012, pp. 139–143.

[17] S. A. Khajehoddin, M. Karimi-Ghartemani, P. K. Jain, and A. Bakhshai, "DC-bus design and control for a single-phase grid-connected renewable converter with a small energy storage component," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3245–3254, Jul. 2013.

[18] T. P. Parker, "Reliability in PV inverter design: Black art or science-based discipline?" Solar Bridge Technol., Austin, TX, USA, White Paper Rev. 1.0, May 2011.

[19] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[20] W. Wang, X. Ruan, and X. Wang, "A novel second harmonic current reduction method for dual active bridge used in photovoltaic power system," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 1635–1639.

[21] S. K. Mazumder, R. K. Burra, and K. Acharya, "A ripple-mitigating and energy-efficient fuel cell power-conditioning system," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1437–1452, Jul. 2007.

[22] R. S. Gemmen, "Analysis for the effect of inverter ripple current on fuel cell operating condition," *J. Fluids Eng.*, vol. 125, no. 3, pp. 576–585, May 2003.

[23] M. Arias, M. Fernández Diaz, D. G. Lamar, D. Balocco, A. A. Diallo, and J. Sebastián, "High-efficiency asymmetrical half-bridge converter without electrolytic capacitor for low-output-voltage AC–DC LED drivers," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2539–2550, May 2013.

[24] J. A. Veitch and S. L. McColl, "Modulation of fluorescent light: Flicker rate and light source effects on visual performance and visual comfort," *Lighting Res. Technol.*, vol. 27, no. 4, pp. 243–256, Dec. 1995.

[25] C. R. Sullivan, J. J. Awerbuch, and A. M. Latham, "Decrease in photovoltaic power output from ripple: Simple general calculation and the effect of partial shading," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 740–747, Feb. 2013.

[26] A. Darwish, S. Alotaibi, and M. A. Elgenedy, "Current-source single-phase module integrated inverters for pv grid-connected applications," *IEEE Access*, vol. 8, pp. 53082–53096, 2020.

[27] Y. Shi, R. Li, Y. Xue, and H. Li, "High-frequency-link-based grid-tied PV system with small DC-link capacitor and low-frequency ripple-free maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 328–339, Jan. 2016.

[28] J. He, Y. W. Li, and F. Blaabjerg, "Flexible microgrid power quality enhancement using adaptive hybrid voltage and current controller," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2784–2794, Jun. 2014.

[29] (2011). *Aluminum Electrolytic Capacitor Application Guide*. [Online]. Available: https://www.cde.com/resources/catalogs/AEappGUIDE.pdf

[30] *Fuel Cell Handbook*, 7th ed., EG&G Tech. Services, Gaithersburg, MD, USA, 2016.

[31] A. Wilkins, J. Veitch, and B. Lehman, "LED lighting flicker and potential health concerns: IEEE standard PAR1789 update," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2010, pp. 171–178.

[32] P. Fang, Y.-F. Liu, and P. C. Sen, "A flicker-free single-stage offline LED driver with high power factor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 654–665, Sep. 2015.

[33] L. Zhang, X. Ruan, and X. Ren, "Second-harmonic current reduction and dynamic performance improvement in the two-stage inverters: An output impedance perspective," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 394–404, Jan. 2015.

[34] J.-M. Kwon, E.-H. Kim, B.-H. Kwon, and K.-H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 826–834, Mar. 2009.

[35] L. Zhang, X. Ren, X. Ruan, and Q. Chen, "Control strategy for the front-end DC-DC converter to reduce the second-order harmonic current in the two-stage inverter," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2013, pp. 719–726.

[36] J. Rodriguez, J.-S. Lai, and F. Zheng Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[37] Z. Wenyi and W. Chen, "Research on voltage-source PWM inverter based on state analysis method," in *Proc. Int. Conf. Mechatronics Autom.*, Aug. 2009, pp. 2183–2187.
[38] M.-K. Nguyen and Y.-O. Choi, "PWM control scheme for quasi-switched-boost inverter to improve modulation index," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4037–4044, May 2018.
[39] M. Liserre, A. Pigazo, A. Dell'Aquila, and V. M. Moreno, "An anti-islanding method for single-phase inverters based on a grid voltage sensorless control," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1418–1426, Oct. 2006.
[40] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.
[41] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010.
[42] A. C. Kyritsis, N. P. Papanikolaou, E. C. Tatakis, and J. C. Kobougias, "Design and control of a current source flyback inverter for decentralized grid-connected photovoltaic systems," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2005, p. 10.
[43] R. L. Steigerwald, "Power electronic converter technology," *Proc. IEEE*, vol. 89, no. 6, pp. 890–897, Jun. 2001.
[44] C.-M. Wang, "A novel single-stage full-bridge buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 150–159, Jan. 2004.
[45] K. Fukushima, I. Norigoe, M. Shoyama, T. Ninomiya, Y. Harada, and K. Tsukakoshi, "Input current-ripple consideration for the pulse-link DC-AC converter for fuel cells by small series LC circuit," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 447–451.
[46] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.
[47] A. Chub, D. Vinnikov, F. Blaabjerg, and F. Z. Peng, "A review of galvanically isolated impedance-source DC–DC converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2808–2828, Apr. 2016.
[48] O. Ellabban and H. Abu-Rub, "Z-source inverter: Topology improvements review," *IEEE Ind. Electron. Mag.*, vol. 10, no. 1, pp. 6–24, Mar. 2016.
[49] S. Vadi, R. Bayindir, and E. Hossain, "A review of control methods on suppression of 2ω ripple for single-phase quasi-Z-source inverter," *IEEE Access*, vol. 8, pp. 42055–42070, 2020.
[50] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.
[51] S. Hu and X. Li, "Performance evaluation of a semi-dual-bridge resonant DC/DC converter with secondary phase-shifted control," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7727–7738, Oct. 2017.
[52] Y. Shen, H. Wang, A. Al-Durra, Z. Qin, and F. Blaabjerg, "A bidirectional resonant DC–DC converter suitable for wide voltage gain range," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2957–2975, Apr. 2018.
[53] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: An overview," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1305–1314, Sep. 2004.
[54] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.
[55] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
[56] S.-J. Jang, C.-Y. Won, B.-K. Lee, and J. Hur, "Fuel cell generation system with a new active clamping current-fed half-bridge converter," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 332–340, Jun. 2007.
[57] V. Mahadeva Iyer and V. John, "Low-frequency DC bus ripple cancellation in single phase pulse-width modulation inverters," *IET Power Electron.*, vol. 8, no. 4, pp. 497–506, Apr. 2015.
[58] G. Zhu, X. Ruan, L. Zhang, and X. Wang, "On the reduction of second harmonic current and improvement of dynamic response for two-stage single-phase inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1028–1041, Feb. 2015.
[59] A. Ale Ahmad, A. Abrishamifar, and S. Samadi, "Low-frequency current ripple reduction in front-end boost converter with single-phase inverter load," *IET Power Electron.*, vol. 5, no. 9, pp. 1676–1683, Nov. 2012.
[60] A. Jamatia, V. Gautam, and P. Sensarma, "Single phase buck-boost derived PV micro-inverter with power decoupling capability," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst. (PEDES)*, Dec. 2016, pp. 1–6.
[61] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.
[62] B. Ge, Y. Liu, H. Abu-Rub, R. S. Balog, F. Z. Peng, S. McConnell, and X. Li, "Current ripple damping control to minimize impedance network for single-phase quasi-Z source inverter system," *IEEE Trans. Ind. Informat.*, vol. 12, no. 3, pp. 1043–1054, Jun. 2016.
[63] B. Ge, Y. Liu, H. Abu-Rub, R. S. Balog, F. Zheng Peng, H. Sun, and X. Li, "An active filter method to eliminate DC-side low-frequency power for a single-phase quasi-Z-Source inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4838–4848, Aug. 2016.
[64] Y. Zhou, H. Li, and H. Li, "A single-phase PV quasi-Z-source inverter with reduced capacitance using modified modulation and double-frequency ripple suppression control," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2166–2173, Mar. 2016.
[65] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected AC-PV modules," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2007, pp. 1–10.
[66] W. Cai, B. Liu, S. Duan, and L. Jiang, "An active low-frequency ripple control method based on the virtual capacitor concept for BIPV systems," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1733–1745, Apr. 2014.
[67] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.
[68] D. Neumayr, G. C. Knabben, E. Varescon, D. Bortis, and J. W. Kolar, "Comparative evaluation of a full-and partial-power processing active power buffer for ultra-compact single-phase DC/AC converter systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Apr. 14, 2020, doi: 10.1109/JESTPE.2020.2987937.
[69] G. C. Christidis, A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "Investigation of parallel active Filters' limitations for power decoupling on single-stage/single-phase microinverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1096–1106, Sep. 2016.
[70] Y. Tang, Z. Qin, F. Blaabjerg, and P. C. Loh, "A dual voltage control strategy for single-phase PWM converters with power decoupling function," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7060–7071, Dec. 2015.
[71] K.-P. Huang, Y. Wang, and R.-J. Wai, "Design of power decoupling strategy for single-phase grid-connected inverter under nonideal power grid," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2938–2955, Mar. 2019.
[72] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 89–95.
[73] H. Zhang, X. Li, B. Ge, and R. S. Balog, "Capacitance, DC voltage utilizaton, and current stress: Comparison of double-line frequency ripple power decoupling for single-phase systems," *IEEE Ind. Electron. Mag.*, vol. 11, no. 3, pp. 37–49, Sep. 2017.
[74] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1855–1865, Apr. 2015.
[75] H. Wang, H. S.-H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the DC-link capacitance in a capacitor-supported system," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1163–1175, Mar. 2014.
[76] X. Lyu, N. Ren, Y. Li, and D. Cao, "A SiC-based high power density single-phase inverter with in-series and in-parallel power decoupling method," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 893–901, Sep. 2016.
[77] W. Liu, K. Wang, H. S.-H. Chung, and S. T.-H. Chuang, "Modeling and design of series voltage compensator for reduction of DC-link capacitance in grid-tie solar inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2534–2548, May 2015.
[78] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "Power decoupling techniques for micro-inverters in PV systems—A review," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2010, pp. 3235–3240.

[79] S. Fan, Y. Xue, and K. Zhang, "A novel active power decoupling method for single-phase photovoltaic or energy storage applications," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2012, pp. 2439–2446.

[80] J.-I. Itoh, T. Sakuraba, K. Kusaka, H. Watanabe, and K. Furukawa, "Comparison of circuit topologies for active power decoupling toward high power density," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, May 2016, pp. 421–428.

[81] H. Watanabe, T. Sakuraba, K. Furukawa, K. Kusaka, and J.-I. Itoh, "Development of DC to single-phase AC voltage source inverter with active power decoupling based on flying capacitor DC/DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4992–5004, Jun. 2018.

[82] R.-J. Wai and C.-Y. Lin, "Active low-frequency ripple control for clean-energy power-conditioning mechanism," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3780–3792, Nov. 2010.

[83] S. Harb, M. Mirjafari, and R. S. Balog, "Ripple-port module-integrated inverter for grid-connected PV applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2692–2698, Nov. 2013.

[84] D. D.-C. Lu, "Comparison of DC/DC converters in DCM for reducing low-frequency input current ripple of single-phase two-stage inverters," in *Proc. 20th Int. Conf. Electr. Mach. Syst. (ICEMS)*, Aug. 2017, pp. 1–4.

[85] S. A. Singh, N. A. Azeez, and S. S. Williamson, "Capacitance reduction in a single phase quasi Z-source inverter using a hysteresis current controlled active power filter," in *Proc. IEEE 25th Int. Symp. Ind. Electron. (ISIE)*, Jun. 2016, pp. 805–810.

[86] Y. Liu, B. Ge, and H. Abu-Rub, "A model predictive control for low-frequency ripple power elimination of active power filter integrated single-phase quasi-Z-source inverter," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Mar. 2017, pp. 1540–1545.

[87] W. Liang, Y. Liu, B. Ge, H. Abu-Rub, R. S. Balog, and Y. Xue, "Double-line-frequency ripple model, analysis, and impedance design for energy-stored single-phase quasi-Z-source photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3198–3209, Apr. 2018.

[88] P. Nandi and R. Adda, "Integration of boost-type active power decoupling topology with single-phase switched boost inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11965–11975, Nov. 2020.

[89] H. B. Dave, D. Singh, and H. O. Bansal, "Multiple linear regression-based impact analysis of impedance network design on life expectancy of DC-link capacitor in q-ZSI fed motor drive," *Eng. Sci. Technol., Int. J.*, 2020, doi: 10.1016/j.jestch.2020.06.004.

[90] G.-R. Zhu, S.-C. Tan, Y. Chen, and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 779–792, Feb. 2013.

[91] G.-R. Zhu, H. Wang, B. Liang, S.-C. Tan, and J. Jiang, "Enhanced single-phase full-bridge inverter with minimal low-frequency current ripple," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 937–943, Feb. 2016.

[92] R. Chen, Y. Liu, and F. Z. Peng, "DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499–5507, Oct. 2015.

[93] S. Bhowmick and L. Umanand, "Design and analysis of the low device stress active power decoupling for single-phase grid connection for a wide range of power factor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1921–1931, Dec. 2018.

[94] A. S. Morsy and P. N. Enjeti, "Comparison of active power decoupling methods for high-power-density single-phase inverters using wide-bandgap FETs for Google little box challenge," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 790–798, Sep. 2016.

[95] J. Roy, Y. Xia, and R. Ayyanar, "Half-bridge voltage swing inverter with active power decoupling for single-phase PV systems supporting wide power factor range," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7450–7461, Aug. 2019.

[96] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1419–1429, Sep. 2000.

[97] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[98] J.-I. Itoh and F. Hayashi, "Ripple current reduction of a fuel cell for a single-phase isolated converter using a DC active filter with a center tap," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 550–556, Mar. 2010.

[99] Y. Liu, B. Ge, H. Abu-Rub, H. Sun, F. Z. Peng, and Y. Xue, "Model predictive direct power control for active power decoupled single-phase quasi-Z-source inverter," *IEEE Trans. Ind. Informat.*, vol. 12, no. 4, pp. 1550–1559, Aug. 2016.

[100] Y. Hu, W. Xiao, W. Cao, Y. Du, and S. Finney, "DC-link voltage control strategy for reducing capacitance and total harmonic distortion in single-phase grid-connected photovoltaic inverters," *IET Power Electron.*, vol. 8, no. 8, pp. 1386–1393, Aug. 2015.

[101] M.-K. Nguyen, T.-D. Duong, Y.-C. Lim, and J.-H. Choi, "High voltage gain quasi-switched boost inverters with low input current ripple," *IEEE Trans. Ind. Informat.*, vol. 15, no. 9, pp. 4857–4866, Sep. 2019.

[102] H. B. Dave, D. Singh, and H. O. Bansal, "High voltage gain reduced current ripple switched coupled inductor quasi-Z-source inverter," *Int. Trans. Electr. Energy Syst.*, vol. 30, no. 4, Apr. 2020.

[103] H. B. Dave, D. Singh, and H. O. Bansal, "Two modified Z-source inverter topologies: A solution to the issues of start-up dc-link voltage overshoot and source current ripple," *J. Power Electron.*, vol. 19, no. 6, pp. 1351–1365, 2019.

[104] *IEEE Draft Recommended Practices and Requirements for Harmonic Control in Electric Power Systems*, IEEE Standard P519/D6ba, Nov. 2013, pp. 1–26.

[105] H.-J. Jung, K.-S. Ha, B.-M. Song, J.-S. Lai, D.-S. Hyun, and R.-Y. Kim, "Low frequency current reduction using a quasi-notch filter operated in two-stage DC–DC–AC grid-connected systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 2746–2750.

[106] C. Liu and J.-S. Lai, "Low frequency current ripple reduction technique with active control in a fuel cell power system with inverter load," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1429–1436, Jul. 2007.

[107] A. R. Gautam, D. Fulwani, R. R. Makineni, and N. Rathore, "ISMC for boost-derived DC–DC–AC converter: Mitigation of 2ω-ripple and uncertainty, and improvement in dynamic performance," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4353–4364, Apr. 2020.

[108] J. Wang, B. Ji, X. Lu, X. Deng, F. Zhang, and C. Gong, "Steady-state and dynamic input current low-frequency ripple evaluation and reduction in two-stage single-phase inverters with back current gain model," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4247–4260, Aug. 2014.

[109] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE Conf. Rec. Annu. Meeting Ind. Appl. Soc.*, vol. 11, 1976, pp. 366–382.

[110] A. Aldhaheri and A. Etemadi, "Impedance decoupling in DC distributed systems to maintain stability and dynamic performance," *Energies*, vol. 10, no. 4, p. 470, Apr. 2017.

[111] R. Bojoi, C. Pica, D. Roiu, and A. Tenconi, "New DC-DC converter with reduced low-frequency current ripple for fuel cell in single-phase distributed generation," in *Proc. IEEE Int. Conf. Ind. Technol.*, Mar. 2010, pp. 1213–1218.

[112] P. F. Ksiazek and M. Ordonez, "Swinging bus technique for ripple current elimination in fuel cell power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 170–178, Jan. 2014.

[113] F. Chen, R. Burgos, D. Boroyevich, and D. Dong, "Control loop design of a two-stage bidirectional AC/DC converter for renewable energy systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 2177–2183.

[114] B. Gu, J. Dominic, J. Zhang, L. Zhang, B. Chen, and J.-S. Lai, "Control of electrolyte-free microinverter with improved MPPT performance and grid current quality," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 1788–1792.

[115] L. Zhang, X. Ren, and X. Ruan, "A bandpass filter incorporated into the inductor current feedback path for improving dynamic performance of the front-end DC-DC converter in two-stage inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2316–2325, May 2014.

[116] H.-C. Chiang, K.-F. Chen, J.-K. Chang, K.-C. Liu, F.-J. Lin, and Y.-L. Chen, "Control method for improving the response of single-phase continuous conduction mode boost power factor correction converter," *IET Power Electron.*, vol. 9, no. 9, pp. 1792–1800, Jul. 2016.

[117] L. Zhang, X. Ruan, and X. Ren, "Second-harmonic current reduction for two-stage inverter with boost-derived front-end converter: Control schemes and design considerations," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6361–6378, Jul. 2018.

[118] B. Liu, L. Wang, D. Song, M. Su, J. Yang, D. He, Z. Chen, and S. Song, "Control of single-phase grid-connected photovoltaic inverter under battery input condition in residential photovoltaic/battery systems," *IEEE Trans. Sustain. Energy*, to be published.

[119] A. H. Mitwalli, S. B. Leeb, G. C. Verghese, and V. J. Thottuvelil, "An adaptive digital controller for a unity power factor converter," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 374–382, Mar. 1996.
[120] A. Prodic, J. Chen, D. Maksimovic, and R. W. Erickson, "Self-tuning digitally controlled low-harmonic rectifier having fast dynamic response," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 420–428, Jan. 2003.
[121] Y. Shi, B. Liu, and S. Duan, "Low-frequency input current ripple reduction based on load current feedforward in a two-stage single-phase inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7972–7985, Nov. 2016.
[122] V. Vlatkovic, J. A. Sabate, R. B. Ridley, F. C. Lee, and B. H. Cho, "Small-signal analysis of the phase-shifted PWM converter," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 128–135, Jan. 1992.
[123] R. Redl and N. O. Sokal, "Near-optimum dynamic regulation of DC-DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. Power Electron.*, vol. PE-1, no. 3, pp. 181–192, Jul. 1986.
[124] X. Liu, H. Li, and Z. Wang, "A fuel cell power conditioning system with low-frequency ripple-free input current using a control-oriented power pulsation decoupling strategy," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 159–169, Jan. 2014.
[125] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proc.-Electr. Power Appl.*, vol. 153, no. 5, pp. 750–762, Sep. 2006.
[126] L. Xue, Z. Shen, D. Boroyevich, P. Mattavelli, and D. Diaz, "Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.
[127] Y. Shi, B. Liu, and S. Duan, "Modelling, control and performance analysis of a single-stage single-phase inverter with reduced low-frequency input current ripple," *IET Power Electron.*, vol. 11, no. 6, pp. 1074–1082, May 2018.
[128] J. M. Galvez and M. Ordonez, "Swinging bus operation of inverters for fuel cell applications with small DC-link capacitance," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1064–1075, Feb. 2015.
[129] G. Bartolini, A. Ferrara, E. Usai, and V. I. Utkin, "On multi-input chattering-free second-order sliding mode control," *IEEE Trans. Autom. Control*, vol. 45, no. 9, pp. 1711–1717, Sep. 2000.
[130] A. R. Gautam, K. Gourav, J. M. Guerrero, and D. M. Fulwani, "Ripple mitigation with improved line-load transients response in a two-stage DC–DC–AC converter: Adaptive SMC approach," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3125–3135, Apr. 2018.
[131] A. R. Gautam and D. Fulwani, "Adaptive SMC for the second-order harmonic ripple mitigation: A solution for the micro-inverter applications," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 8254–8264, Aug. 2019.
[132] S. Bayhan and H. Komurcugil, "A sliding-mode controlled single-phase grid-connected quasi-Z-source npc inverter with double-line frequency ripple suppression," *IEEE Access*, vol. 7, pp. 160004–160016, 2019.
[133] L. Zhang, X. Ruan, and X. Ren, "One-cycle control for electrolytic capacitor-less second harmonic current compensator," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1724–1739, Feb. 2018.
[134] M. Mellincovsky, V. Yuhimenko, M. M. Peretz, and A. Kuperman, "Low-frequency DC-link ripple elimination in power converters with reduced capacitance by multiresonant direct voltage regulation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2015–2023, Mar. 2017.
[135] M. Mellincovsky, V. Yuhimenko, Q. C. Zhong, M. M. Peretz, and A. Kuperman, "Active DC link capacitance reduction in grid-connected power conversion systems by direct voltage regulation," *IEEE Access*, vol. 6, pp. 18163–18173, 2018.
[136] R.-J. Wai and C.-Y. Lin, "Dual active low-frequency ripple control for clean-energy power-conditioning mechanism," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5172–5185, Nov. 2011.
[137] H. Watanabe and J.-I. Itoh, "Isolated single-phase AC grid connected converter with small inductors and capacitors for micro-inverters," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2017, pp. 1542–1549.
[138] M. Chen, Z. Ye, Y. Chen, and D. Xu, "Zero-voltage-switching single-phase full-bridge inverter with active power decoupling," *IEEE Trans. Power Electron.*, early access, May 29, 2020, doi: 10.1109/TPEL.2020.2998640.
[139] W. Yao, X. Wang, X. Zhang, Y. Tang, P. C. Loh, and F. Blaabjerg, "A unified active damping control for single-phase differential mode buck inverter with LCL-filter," in *Proc. IEEE 6th Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2015, pp. 1–8.
[140] S. Xu, R. Shao, L. Chang, and M. Mao, "Single-phase differential buck–boost inverter with pulse energy modulation and power decoupling control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2060–2072, Dec. 2018.
[141] R. O. Caceres and I. Barbi, "A boost DC-AC converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, Jan. 1999.
[142] Y. Xia, J. Roy, and R. Ayyanar, "A single phase doubly grounded, PV inverter using coupled inductor with integrated magnetics and active power decoupling technique," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2017, pp. 8–14.
[143] X. Liu, P. Wang, P. C. Loh, F. Blaabjerg, and M. Xue, "Six switches solution for single-phase AC/DC/AC converter with capability of second-order power mitigation in DC-link capacitor," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 1368–1375.
[144] Y. Liu, M. Su, F. Liu, M. Zheng, X. Liang, G. Xu, and Y. Sun, "Single-phase inverter with wide input voltage and power decoupling capability," *IEEE Access*, vol. 7, pp. 16870–16879, 2019.
[145] Y. Ohnuma, K. Orikawa, and J.-I. Itoh, "A single-phase current-source PV inverter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 531–538, Jan. 2015.
[146] A. Jamatia, V. Gautam, and P. Sensarma, "Power decoupling method for single phase PV system using uk derived micro-inverter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2016, pp. 1–7.
[147] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an AC photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.
[148] W. Yao, Y. Xu, Y. Tang, P. C. Loh, X. Zhang, and F. Blaabjerg, "Generalized power decoupling control for single-phase differential inverters with nonlinear loads," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1137–1151, Jun. 2019.
[149] M. Jang and V. G. Agelidis, "A minimum power-processing stage fuel cell energy system based on a boost-inverter with a bi-directional back-up battery storage," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2010, pp. 295–302.
[150] D. B. W. Abeywardana, B. Hredzak, and V. G. Agelidis, "A rule-based controller to mitigate DC-side second-order harmonic current in a single-phase boost inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1665–1679, Feb. 2016.
[151] D. B. W. Abeywardana, B. Hredzak, and V. G. Agelidis, "An input current feedback method to mitigate the DC-side low-frequency ripple current in a single-phase boost inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4594–4603, Jun. 2016.
[152] E. Makovenko, O. Husev, J. Zakis, C. Roncero-Clemente, E. Romero-Cadaval, and D. Vinnikov, "Passive power decoupling approach for three-level single-phase impedance source inverter based on resonant and PID controllers," in *Proc. 11th IEEE Int. Conf. Compat., Power Electron. Power Eng. (CPE-POWERENG)*, Apr. 2017, pp. 516–521.

ADITYA R. GAUTAM (Member, IEEE) received the B.Tech. and M.Tech. degrees from the National Institute of Technology (NIT) Bhopal, India, in 2011 and 2013, respectively, and the Ph.D. degree from the Department of Electrical Engineering, IIT Jodhpur, India, in 2019. He is currently an Assistant Professor with the Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science, Pilani, India. His current research interests include nonlinear control of power converters, microgrid, and electric vehicles.

DEEPAK M. FULWANI (Member, IEEE) received the Ph.D. degree from IIT Bombay, in 2009. He was with IIT Guwahati and IIT Kharagpur. He is currently an Associate Professor with the Department of Electrical Engineering, IIT Jodhpur. His research interests include control of networked systems and dc microgrid.

RAMMOHAN R. MAKINENI received the B.E. degree in electrical and electronics engineering from Andhra University, India, in 2011, and the M.E. degree in power electronics and drives from the PEC University of Technology, Chandigarh, India, in 2013. He is currently a Research Fellow at IIT Jodhpur. His research interests include control, power electronics, electrical drives, microgrid, and electric vehicles.

AKSHAY KUMAR RATHORE (Senior Member, IEEE) received the Ph.D. degree in power electronics from the University of Victoria, Victoria, BC, Canada, in 2008. He had two postdoctoral research appointments with the University of Wuppertal, Germany, and with the University of Illinois at Chicago, USA. He was an Assistant Professor with the Department of Electrical and Computer Engineering, National University of Singapore. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, Concordia University, Montreal, QC, Canada. His research interests include current-fed converters and multilevel inverters. He is currently a prominent Lecturer and an Awards Department Chair of the IEEE Industry Applications Society. He has been with several technical committees and with conference organizing committees in various roles.

DHEERENDRA SINGH (Senior Member, IEEE) received the B.E. degree in electrical engineering from IIT Roorkee (formerly University of Roorkee), the M.Tech. degree from IIT Delhi, and the Ph.D. degree in power quality from BITS-Pilani. He has more than 25 years of teaching and industrial experience. He has supervised one doctoral thesis and more than 100 postgraduate/undergraduate research projects. He has authored approximately 30 research articles in reputed journals and conferences. He is currently involved in teaching and research in the area of power electronics-based renewable energy systems, controls and drives, application of AI techniques, and the IoT. He is a Life Member of IETE, India. He successfully coordinated many graduate programs for the industries, such as National Thermal Power Corporation (NTPC), Chambal Fertilizers and Chemical Ltd. (CFCl), and Hindustan Zinc.