AIP Journal of Applied Physics

Study of electrical performance and stability of solution-processed n -channel organic field-effect transistors

Shree Prakash Tiwari, Xiao-Hong Zhang, William J. Potscavage Jr., and Bernard Kippelen

Citation: Journal of Applied Physics **106**, 054504 (2009); doi: 10.1063/1.3204655
View online: http://dx.doi.org/10.1063/1.3204655
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/106/5?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

Hole mobility enhancement of pentacene organic field-effect transistors using 4,4′,4″-tris[3-methylphenyl(phenyl)amino] triphenylamine as a hole injection interlayer
Appl. Phys. Lett. **99**, 063306 (2011); 10.1063/1.3624586

Improved n-type bottom-contact organic transistors by introducing a poly(3,4-ethylenedioxythiophene):poly(4-styrene sulfonate) coating on the source/drain electrodes
Appl. Phys. Lett. **97**, 103304 (2010); 10.1063/1.3488817

Low-voltage solution-processed n-channel organic field-effect transistors with high- k HfO 2 gate dielectrics grown by atomic layer deposition
Appl. Phys. Lett. **95**, 223303 (2009); 10.1063/1.3269579

Integration of reduced graphene oxide into organic field-effect transistors as conducting electrodes and as a metal modification layer
Appl. Phys. Lett. **95**, 023304 (2009); 10.1063/1.3176216

Conducting channel formation and annihilation in organic field-effect structures
J. Appl. Phys. **105**, 024514 (2009); 10.1063/1.3068189

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 128.193.164.203 On: Sun, 21 Dec 2014 07:41:09

Study of electrical performance and stability of solution-processed *n*-channel organic field-effect transistors

Shree Prakash Tiwari, Xiao-Hong Zhang, William J. Potscavage, Jr., and Bernard Kippelen[a)]
Center for Organic Photonics and Electronics (COPE), School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332, USA

(Received 13 May 2009; accepted 14 July 2009; published online 2 September 2009)

Solution processed *n*-channel organic field-effect transistors based on [6,6]-phenyl C_{61} butyric acid methyl ester with high mobility and low contact resistance are reported. Ca, Au, or Ca capped with Au (Ca/Au) was used as the top source/drain electrodes. The devices with Ca electrodes exhibit excellent *n*-channel behavior with electron mobility values of $0.12\ cm^2/V\ s$, low threshold voltages (~ 2.2 V), high current on/off ratios (10^5-10^6) and subthreshold slopes of 0.7 V/decade. By varying the channel lengths (25–200 μm) in devices with different metal/semiconductor interfaces, the effect of channel length scaling on mobility is studied and the contact resistance is extracted. The width-normalized contact resistance ($R_C W$) for Au (12 kΩ cm) is high in comparison to Ca (7.2 kΩ cm) or Ca/Au (7.5 kΩ cm) electrodes at low gate voltage ($V_{GS}=10$ V). However, in the strong accumulation regime at high gate voltage ($V_{GS}=30$ V), its value is nearly independent of the choice of metal electrodes and in a range of 2.2–2.6 kΩ cm. These devices show stable electrical behavior under multiple scans and low threshold voltage instability under electrical bias stress ($V_{DS}=V_{GS}=30$ V, 1 h) in N_2 atmosphere. © *2009 American Institute of Physics*.
[doi:10.1063/1.3204655]

I. INTRODUCTION

Organic field-effect transistors (OFETs) are receiving significant attention because of their potential application for low-cost, flexible electronics, such as displays, smart pixels, and radio frequency identification tags.[1–3] As one step toward achieving this goal, organic complementary logic circuits based on *p*- and *n*-channel organic transistors fabricated by vacuum evaporation have been reported.[4,5] In *n*-channel devices with fullerene molecules processed by vacuum deposition,[6] field-effect mobility values up to $6\ cm^2/V\ s$ have been reported. To take advantage of large-area and low-cost processing, solution-processed OFETs are preferred. Solution-processed *p*-channel OFETs[7,8] with saturation mobility values up to $0.7\ cm^2/V\ s$ and solution-processed *n*-channel OFETs[9] with electron mobility values up to $0.85\ cm^2/V\ s$ have been reported recently. Despite these advances in new materials, comprehensive studies of the influence of the choice of electrodes on the performance and stability of OFETs remain relatively scarce.[10–13]

Here, we report on solution-processed *n*-channel OFETs based on [6,6]-phenyl C_{61} butyric acid methyl ester with different metal source/drain electrodes [Ca, Au, or Ca capped with Au (Ca/Au)] with varying channel lengths (25–200 μm). Among electron transport materials, fullerene-based compounds are known to be promising candidates for solution-processed *n*-channel OFETs.[14–18] [6,6]-phenyl C_{61} butyric acid methyl ester ([60]PCBM) is a widely studied fullerene based compound[15–19] and will serve in this study as a model material for the investigation of electron injection from different electrodes. A top-contact configuration with Ca, Au, and Ca capped by Au (Ca/Au) as source and drain (S/D) electrodes is used with divinyltetramethyldisiloxanebis(benzocyclobutene) (BCB) on top of thermally grown SiO_2 as the gate dielectric layer. BCB was chosen to minimize electron trapping at the dielectric/semiconductor interface, which is a primary limiting factor for *n*-channel conduction.[20,21] The devices with Ca/Au were fabricated to study the stability of these devices upon exposure to normal ambient. We also investigate the stability of these devices under multiple transfer characteristics scans and under continuous electrical bias stress. Threshold voltage instability and degradation upon exposure to ambient are also discussed.

II. EXPERIMENTS

OFETs in a top-contact configuration were fabricated on heavily *n*-doped (n^+) silicon substrates (resistivity $<0.005\ \Omega$ cm with a wafer thickness of $525 \pm 15\ \mu$m from Silicon Quest Int.), which also serve as the gate electrodes, with 200-nm-thick thermally grown SiO_2 as the gate dielectric (Fig. 1). Ti/Au (10 nm/100 nm) metallization on the backside of the substrate was done after removing the backside SiO_2 layer with a buffered oxide etchant to enhance the gate electrical contact. The substrates were cleaned with air plasma for 3 min to make the SiO_2 surface hydrophilic and ensure good film formation. The substrates were immediately loaded into a N_2-filled glovebox where the rest of the fabrication processes were performed. The SiO_2 dielectric surface was then passivated with a thin buffer layer of BCB. The BCB (Cyclotene™, Dow Chemicals) was diluted in trimethylbenzene with a ratio of 1:20 and spin coated at 3000 rpm

[a)]Author to whom correspondence should be addressed. Electronic address: kippelen@ece.gatech.edu.

 © 2009 American Institute of Physics

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 128.193.164.203 On: Sun, 21 Dec 2014 07:41:09

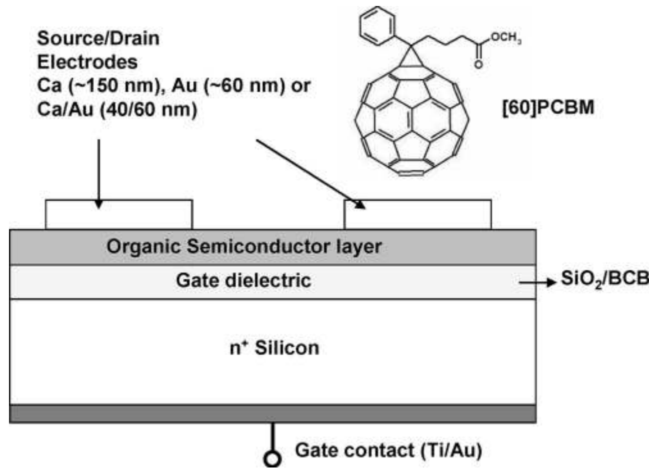

FIG. 1. Device structure of a top contact OFET along with the chemical structure of [60]PCBM.

for 60 s to deposit a very thin and uniform layer. The samples were annealed at 250 °C for 1 h inside the N_2 glovebox for crosslinking. The total capacitance density (C_{OX}) measured from parallel-plate capacitors of various areas was ~13.9 nF/cm^2. A thin layer of [60]PCBM (Solenne B.V., 99.5 %) was deposited on the substrates by spin coating from a solution in chlorobenzene (10 mg/ml) at 1000 rpm for 60 s. [60]PCBM was never exposed to normal ambient during the fabrication process.

Ideally, the work function of the S/D electrodes should match the lowest unoccupied molecular orbital (LUMO) level of an electron transport organic semiconductor to provide a low injection barrier for electrons. Thus, Ca (work function 2.9 eV) S/D electrodes were chosen for the *n*-channel operation in [60]PCBM (LUMO ~3.5 eV). A 150-nm-thick Ca layer was deposited through a shadow mask to act as the top S/D electrodes with channel lengths ranging from L=25 to 200 μm. However, Ca electrodes oxidize easily in the presence of moisture and oxygen to form a nonconducting oxide. Since Au electrodes are more stable, devices with Au (60 nm) S/D electrodes were also fabricated; however, due to its high work function of ~5.1 eV, Au creates a large barrier for injection of electrons into [60]PCBM. Therefore, devices with Ca capped by Au (Ca/Au 40/60 nm) were fabricated to study the stability of the devices upon exposure to normal ambient. These devices will have the advantage of a [60]PCBM/Ca interface with a low injection barrier for electrons as well as a stable layer of Au to protect the Ca from normal ambient and prevent oxidation.

The samples were transferred in a vacuum-tight vessel without being exposed to atmospheric conditions into another N_2-filled glovebox (O_2, H_2O ~ 0.1 ppm) for electrical testing. The electrical measurements were performed using an Agilent E5272A source/monitor unit connected to a computer. Output (I_{DS} versus V_{DS}) and transfer (I_{DS} versus V_{GS}) characteristics were measured (dwell time=20 to 50 s, integration time=6×80 μs^2) for devices with channel lengths from 200 to 25 μm. Field-effect mobility (μ) values and threshold voltages (V_{TH}) were measured in the saturation regime from the highest slope of $|I_{DS}|^{1/2}$ versus V_{GS} plots using the saturation region current equation

TABLE I. Summary of the electrical parameters for [60]PCBM transistors: field-effect mobility in the saturation region (μ), threshold voltage (V_{TH}), on/off current ratio ($I_{on/off}$), and subthreshold slope (SS).

Device (W/L)	μ (cm^2/V s)	V_{TH} (V)	$I_{on/off}$	SS (V/dec)
Ca (~150 nm) S/D electrode				
1000 μm/25 μm (4 dev.)	0.11(±0.02)	2.1(±0.2)	1×10^6	0.9
1000 μm/50 μm (3 dev.)	0.11(±0.02)	2.6(±0.3)	2×10^5	0.9
1000 μm/100 μm (4 dev.)	0.12(±0.03)	2.2(±0.2)	5×10^5	0.7
1000 μm/200 μm (3 dev.)	0.13(±0.04)	1.7(±0.2)	2×10^5	0.7
Au (~60 nm) S/D electrode				
1000 μm/25 μm (4 dev.)	0.03(±0.01)	5.5(±0.3)	1×10^6	0.9
1000 μm/50 μm (4 dev.)	0.06(±0.01)	5.7(±0.7)	5×10^5	0.8
1000 μm/100 μm (4 dev.)	0.09(±0.01)	5.9(±1.8)	2×10^5	0.8
1000 μm/200 μm (4 dev.)	0.11(±0.02)	5.3(±2.0)	2×10^5	0.7
Ca/Au (~40/60 nm) S/D electrode				
1000 μm/25 μm (4 dev.)	0.103(±0.004)	2.5(±0.2)	2×10^6	0.7
1000 μm/50 μm (4 dev.)	0.103(±0.002)	3.0(±0.3)	1×10^6	0.8
1000 μm/100 μm (4 dev.)	0.114(±0.005)	2.6(±0.5)	1×10^6	0.8
1000 μm/200 μm (4 dev.)	0.123(±0.003)	2.3(±0.3)	5×10^5	0.7

$$I_{DS} = \frac{1}{2}\mu C_i \frac{W}{L}(V_{GS} - V_{TH})^2, \qquad (1)$$

where C_i is the capacitance per unit area of the gate dielectric [F/cm^2], and W (width) and L (length) are the dimensions of the semiconductor channel defined by the source and drain electrodes of the transistor.

To study the operational stability, the devices were repeatedly stressed by measuring transfer characteristics in the saturation regime 100 times with a 2 s waiting time between cycles. For the study of stability under a constant bias, the time-dependent decay of I_{DS} was tested under a dc bias stress of $V_{GS}=V_{DS}$=30 V for 1 h. To study the stability of devices upon exposure to ambient, the devices were transferred back to the N_2 atmosphere for characterization after exposure to normal ambient (30 min).

III. RESULTS AND DISCUSSION

A. Electrical characteristics

Devices with W=1000 μm and various channel lengths (L=25, 50, 100, and 200 μm) having electrodes of Ca, Au, or Ca/Au (14, 16, and 16 devices on a single substrate, respectively) were characterized to obtain the electron mobility (μ), threshold voltage (V_{TH}), current on/off ratio (I_{on}/I_{off}), and subthreshold slope (SS). Table I summarizes the performance parameters for all of the devices with μ and V_{TH} averaged over several devices and $I_{on/off}$ and SS reported for one representative device. Figures 2(a) and 2(b) show the output and transfer characteristics of a representative OFET (W/L=1000 μm/100 μm) with Ca electrodes. The devices with the same dimensions of W/L=1000 μm/100 μm (4 devices) exhibited an average electron mobility of 0.12±0.03 cm^2/V s with an average threshold voltage of 2.2±0.2 V. The current on/off ratios were in the range of 10^5–10^6. The devices showed excellent *n*-channel behavior

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 128.193.164.203 On: Sun, 21 Dec 2014 07:41:09

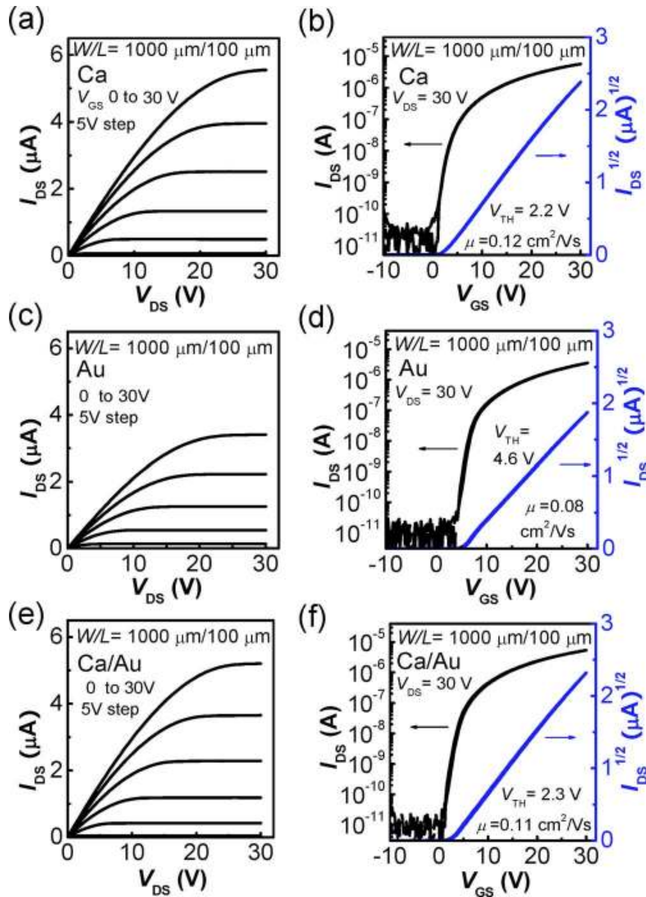

FIG. 2. (Color online) Output and transfer characteristics of [60]PCBM OFETs with Ca [(a) and (b)], Au [(c) and (d)], and Ca/Au [(e) and (f)] source/drain electrodes with device dimensions of $W/L = 1000\ \mu\text{m}/100\ \mu\text{m}$. The average threshold voltages in devices with Au electrodes is high (>2 times) in comparison to devices with Ca or Ca/Au electrodes.

having no hysteresis in the transfer characteristics and SSs of 0.7 V/decade. The subthreshold values reported here are one order lower than values of 7.3 V/decade for [60]PCBM devices on BCB dielectric reported earlier.[17] Devices with larger channel lengths (200 μm) gave a slightly higher saturation mobility ($0.13 \pm 0.04\ \text{cm}^2/\text{V s}$) in comparison to the shorter channel lengths (averaging $0.11 \pm 0.02\ \text{cm}^2/\text{V s}$ for $L = 25\ \mu$m). The maximum field-effect mobility values (μ_{FE}) obtained in the linear regime ($0.12\ \text{cm}^2/\text{V s}$, at $V_{DS} = 3$ V) were also similar to the saturation mobility for $W/L = 1000\ \mu\text{m}/100\ \mu\text{m}$; here, we are referring to saturation mobility values at $V_{DS} = 30$ V for all the results shown in this paper.

Figures 2(c) and 2(d) show the typical output and transfer characteristics of OFETs ($W/L = 1000\ \mu\text{m}/100\ \mu\text{m}$) with Au electrodes. The devices with $W/L = 1000\ \mu\text{m}/100\ \mu\text{m}$ (4 devices) exhibited an average electron mobility of $0.09 \pm 0.01\ \text{cm}^2/\text{V s}$ and higher threshold voltage (5.9 ± 1.8 V). The mobility for these devices (Au electrodes) drops drastically for shorter channel lengths. Devices with dimensions $W/L = 1000\ \mu\text{m}/200\ \mu\text{m}$ (4 devices) exhibited an electron mobility value of $0.11 \pm 0.02\ \text{cm}^2/\text{V s}$, with threshold voltage of 5.3 ± 2.0 V, while the devices with shorter channel lengths ($W/L = 1000\ \mu\text{m}/25\ \mu\text{m}$, 4 devices) exhibited a low average electron mobility value of $0.03 \pm 0.01\ \text{cm}^2/\text{V s}$ with threshold voltage of 5.5 ± 0.3 V. This indicates the dominance of contact resistance in these devices upon scaling down the channel length. However, the current on/off ratios are high ($10^5 - 10^6$) with the SSs of 0.7–0.9 V/decade.

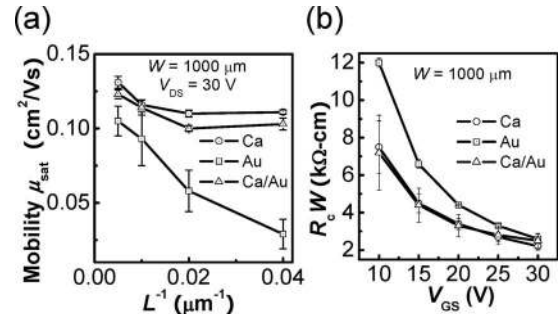

FIG. 3. (a) The dependence of mobility on the inverse of channel length. (b) The width-normalized contact resistance ($R_C W$) obtained from [60]PCBM OFETs with Ca, Au, and Ca/Au source/drain electrodes.

Figures 2(e) and 2(f) show the output and transfer characteristics of an OFET ($W/L = 1000\ \mu\text{m}/100\ \mu\text{m}$) with Ca/Au electrodes. The devices with dimensions of $W/L = 1000\ \mu\text{m}/100\ \mu\text{m}$ (4 devices) exhibited an average electron mobility of $0.114 \pm 0.005\ \text{cm}^2/\text{V s}$ with an average threshold voltage of 2.6 ± 0.5 V. The electron mobility here is slightly lower than the mobility values for the devices with only Ca electrodes. The current on/off ratios for these devices are on the order of 10^6. The devices showed excellent *n*-channel behavior with no hysteresis in the transfer characteristics and SSs of 0.8 V/decade. Similar to the Ca-only devices but with smaller standard deviations, the devices with larger channel lengths (200 μm) provided slightly higher saturation mobility ($0.123 \pm 0.003\ \text{cm}^2/\text{V s}$) in comparison to the shorter channel lengths (averaging $0.103 \pm 0.004\ \text{cm}^2/\text{V s}$ for $W/L = 1000\ \mu\text{m}/25\ \mu\text{m}$). Though these devices have electrical parameters similar to devices with Ca electrodes, the Au capping layer has the advantage of protecting the Ca electrodes against the ambient from the top (as explained in the Sec. III D).

B. Dependence of mobility on the channel length *L* and contact resistance

To investigate the dependence of mobility on the channel length L, field-effect mobility values of devices are statistically plotted over the inverse of channel length (L^{-1}) with a channel width $W = 1000\ \mu$m in Fig. 3(a). As explained in the Sec. III A, the mobility decreases upon scaling the channel lengths from 200 μm down to 25 μm due to the injection barrier at the metal/organic interface, especially in devices with Au electrodes. For a better understanding of the effect of the injection barrier on the mobility, the contact resistance in each type of device was extracted using a transmission line method based on the dependence of the current-voltage characteristics on channel length. A set of devices with channel lengths ranging from $L = 25$ to 100 μm and a fixed channel width of $W = 1000\ \mu$m was used to calculate the contact resistance at a low V_{DS} of 1 V for V_{GS} values ranging from

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 128.193.164.203 On: Sun, 21 Dec 2014 07:41:09

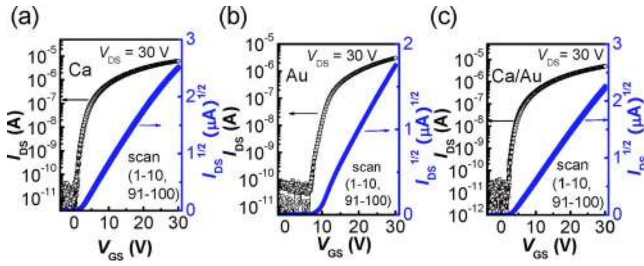

FIG. 4. (Color online) Superimposed transfer characteristics from the first 10 scans and the last 10 scans during a 100 time scan test with 2 s rest time between cycles for a particular device with Ca (a), Au (b), and Ca/Au (c) source/drain electrodes.

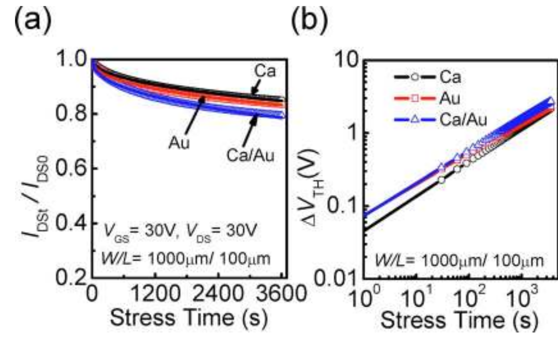

FIG. 5. (Color online) (a) Decay of drain-source current for the stress condition of $V_{GS}=V_{DS}=30$ V over 1 h. The experimental data of this plot is fitted by a stretched exponential curve from Eq. (6). (b) Threshold voltage shift (ΔV_{TH}) was calculated from the fitting parameters extracted from the data in (a).

10 to 30 V. In the linear regime, the overall device resistance R_{on} can be considered to be the sum of the channel resistance R_{ch} and the total contact resistance R_C, as already explained in the literature,[22–25] with

$$R_{on} = \left. \frac{\partial V_{DS}}{\partial I_{DS}} \right|_{V_{DS}\to 0}^{V_{GS}} = R_{ch} + R_C = R_{sh}\frac{L}{W} + R_C, \quad (2)$$

yielding

$$R_{on}W = R_{sh}L + R_C W, \quad (3)$$

where R_{sh} is the sheet resistance of the channel. The R_{on} is calculated in the linear regime ($V_{DS}=1$ V) by dividing the V_{DS} by I_{DS} at V_{GS} values of 10, 15, 20, 25, and 30 V. The width-normalized contact resistance ($R_C W$) was estimated according to Eq. (3) by extrapolating $R_{on}W$ to $L=0$ μm using the y intercept of plots of $R_{on}W$ versus L, and $R_C W$ for different V_{GS} are plotted in Fig. 3(b).

As expected, at a low gate voltage of $V_{GS}=10$ V, the width normalized contact resistance for Au electrodes (12 kΩ cm) is higher in comparison to Ca (7.2 kΩ cm) or Ca/Au (7.5 kΩ cm) electrodes. However, $R_C W$ drops drastically for all three types of electrodes with V_{GS} in the strong accumulation to 2.2, 2.6, and 2.5 kΩ cm for Ca, Au, and Ca/Au, respectively, at a high gate voltage of $V_{GS}=30$ V. This behavior is in agreement with the explanation for contact resistance in the organic field-effect transistors of Ref. 25 and references cited therein. The $R_C W$ values for Au (top contact) in our devices are much lower (4.4 kΩ cm versus 6 MΩ cm at $V_{GS}=20$ V) than the values reported for bottom-contact structures.[19] These results also indicate that the effect of contact resistance will be low at high gate voltages even for Au electrodes, which make a Schottky-like contact to [60]PCBM with a high injection barrier for electrons;[26] however, these type of contacts cannot be used for low voltage applications.

C. Operational stability and bias stress effect

To study the electrical stability of the devices, the transfer characteristics of the devices were first scanned 100 times with a time interval of 2 s between scans in N_2, as mentioned earlier. The superimposed measured transfer curves from the first 10 cycles and the last 10 cycles are shown for the devices with Ca, Au, and Ca/Au electrodes in Figs. 4(a)–4(c), respectively. Here, no significant performance degradation could be observed in the transistors' electrical performance with respect to mobility and threshold voltage. The shape of the successive transfer curves remained almost unchanged during 100 scans. Negligible threshold voltage shift occurred during these scans, indicating good electrical stability and reproducibility for devices under normal operation, resulting in the reliable extraction of device parameters.

Figure 5(a) shows the time-dependent decay of I_{DS} under a dc bias stress with $V_{GS}=V_{DS}=30$ V over 1 h for all three types of devices. The current decay in this experiment exhibited typical features of bias stress instability showing an exponential decay function with 15% to 20% decay in I_{DS} after one hour, where the degradation rate slows with stressing time. The bias stress instability can be modeled by a stretched exponential function fitted to either the threshold voltage shift (ΔV_{TH}) or the drain-source channel current decay. A stretched-exponential equation for ΔV_{TH} was proposed by Libsch and Kanicki as[27]

$$|\Delta V_{TH}(t)| = |V_{GS} - V_{TH0}|\{1 - \exp[-(t/\tau)^{\beta}]\}, \quad (4)$$

where V_{TH0} is the initial threshold voltage at time $t=0$ s. The dispersion parameter β is the stretched exponential factor, reflecting the width of the involved trap distribution, and the constant τ represents the characteristic trapping time of the carriers.

If the term V_{GS} is replaced with $V_{TH}(\infty)$ in the Eq. (4), it is more suitable for OFETs stressed for a very long time;[28,29] however, for a shorter stressing time (1 h), both versions of this equation {with V_{GS} or $V_{TH}(\infty)$} seem equally appropriate to use. This model can be extended to fit the decay of I_{DS} over time under a dc bias stress.[30] Using the decay of I_{DS} instead of the threshold voltage shift to estimate stability can avoid the error and inaccuracy caused by the measurement and extraction of threshold voltage. Based on Eq. (1) for the saturation current, the ratio of the I_{DS} at time t and at 0 s can be written as

$$\frac{I_{DS}(t)}{I_{DS}(0)} = \frac{\{V_{GS} - [V_{TH0} + \Delta V_{TH}(t)]\}^2}{(V_{GS} - V_{TH0})^2}, \quad (5)$$

where $[V_{TH0}+\Delta V_{TH}(t)]$ is the threshold voltage at time t. Combining the stretched-exponential equation for $\Delta V_{TH}(t)$ from Eq. (4) with Eq. (5) results in an equation for the ratio of the I_{DS} at time t and at 0 s as

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 128.193.164.203 On: Sun, 21 Dec 2014 07:41:09

$$\frac{I_{DS}(t)}{I_{DS}(0)} = \exp\left[-2\left(\frac{t}{\tau}\right)^{\beta}\right]. \quad (6)$$

The experimental data from Fig. 5(a) was fitted to Eq. (6), and τ and β values were extracted for all three types of devices. The dispersion parameter β, reflecting the width of the involved trap distribution (at room temperature in this case) was 0.47, 0.43, and 0.44, respectively for the devices with Ca, Au, and Ca/Au. These β values are slightly higher than the values for FETs with amorphous thin-film silicon transistors ($\sim$0.39),[31] solution-processed air stable organic materials ($\sim$0.30),[32] and vacuum-evaporated pentacene on various dielectric surfaces (0.41),[33] at room temperature ($\sim$300 K).

The extracted τ values were in between 10^5 and 10^6 (6.7×10^5, 9.6×10^5, and 4.6×10^5 for Ca, Au, and Ca/Au, respectively). These values lie in the lower range of our recent results obtained with vacuum evaporated pentacene (τ varied from 10^5 to 10^8) on various dielectric surfaces.[31] Using these extracted values, the threshold voltage instability, i.e., ΔV_{TH}, with bias stress time is obtained with the help of Eq. (4) and shown in Fig. 5(b). These results show that, ΔV_{TH} is the lowest for the devices with Ca, and it approaches to 2.2, 2.4, and 2.7 V for devices with Ca, Au, and Ca/Au respectively after a continuous bias stress of $V_{GS}=V_{DS}=30$ V for 1 h. However, this value is within 10% of the device operating voltages or stress voltages for all three types of devices. These results show that these OFETs have relatively good operational and electrical bias stability, which is very important for the reliable operation of organic devices and circuits.

D. Stability study after exposure to normal ambient

As mentioned earlier, the devices with Ca capped by Au (Ca/Au, 40/60 nm) were fabricated to study the stability of the devices upon exposure to normal ambient. These devices have the advantage of a low barrier PCBM/Ca interface for *n*-channel device operation, as well as a stable layer of Au to protect the Ca electrodes from moisture and O_2. To study the stability of devices upon exposure to ambient, all three types of devices were exposed to normal ambient for 30 min and transferred back to N_2 atmosphere for electrical characterization. Figures 6(a) and 6(b) show degradation in the output ($V_{GS}=30$ V) and transfer characteristics before and after 30 min of exposure to ambient for devices with Au electrodes. Figures 6(c) and 6(d) show the degradation in output and transfer characteristics for the devices with Ca/Au electrodes. Table II lists the electrical parameters for the devices before and after exposure to normal ambient. The devices with only Ca electrodes are not shown because they do not show any transistor behavior after exposure.

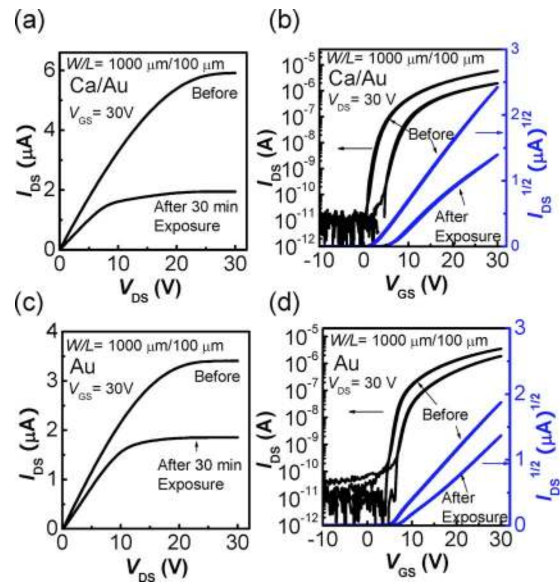

FIG. 6. (Color online) Degradation in the output ($V_{GS}=30$ V) and transfer characteristics after 30 min exposure to ambient: Au electrodes [(a) and (b)] and Ca/Au electrodes [(c) and (d)]. The devices with only Ca electrodes did not show OFET behavior after exposure to air.

There is a degradation of 50% in the electron mobility values for the devices with both Au and Ca/Au electrodes; however, the devices with Au only electrodes show less degradation with respect to the current on/off ratios and the "on" currents (45% drop in I_{on} for devices with Au electrodes versus 67% drop in I_{on} for Ca/Au). The similar drop in electron mobility values for both of the devices indicates that this degradation is probably occurring due to changes in the electronic properties of the organic semiconductor film. However, there is also a possibility of degradation of Ca/Au electrodes due to the penetration of the O_2/H_2O into the Ca layer through the sides. These results show that capping the Ca electrodes with a Au layer provides somewhat improved stability upon exposure to ambient but does not solve the stability issue entirely.

IV. CONCLUSION

The electrical performance and stability of solution-processed *n*-channel OFETs with [60]PCBM was studied in a top-contact configuration using Ca, Au, and Ca/Au source/drain electrodes and SiO_2/BCB as a gate dielectric layer. The

TABLE II. Summary of the electrical parameters for [60]PCBM transistors before and after exposure to normal ambient for 30 min (for the devices with $W/L=1000$ μm/100 μm).

	Before exposure				After exposure (30 min)			
S/D	μ (cm^2/V s)	V_{TH} (V)	I_{on} (μA)	I_{on}/I_{off}	μ (cm^2/V s)	V_{TH} (V)	I_{on} (μA)	I_{on}/I_{off}
Ca	0.12	2.1	5.6	5×10^5	⋯	⋯	0	0
Au	0.08	4.6	3.5	2×10^5	0.04	6.7	1.9	1×10^5
Ca/Au	0.12	2.1	5.9	1×10^6	0.06	5.4	1.9	3×10^5

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 128.193.164.203 On: Sun, 21 Dec 2014 07:41:09

devices with [60]PCBM and Ca S/D electrodes exhibited excellent n-channel behavior with an average electron mobility of about $0.12\ cm^2/V\ s$ and a low threshold voltage of $\sim 2.2\ V$. These OFETs showed high values of current on/off ratios (10^5-10^6) and relatively stable electrical behavior with no hysteresis when tested in an inert environment. The mobility in devices with Au electrodes drops drastically upon scaling the channel length (from $0.12\ cm^2/V\ s$ for $L=200\ \mu m$ to $0.03\ cm^2/V\ s$ for $L=25\ \mu m$). On the other hand, the devices with Ca or Ca/Au electrodes show very low variation in mobility with channel length scaling. Multiple transfer characteristic scans and bias stress studies indicate that these OFETs exhibit excellent reproducibility with low threshold voltage instability when tested in inert atmosphere.

ACKNOWLEDGMENTS

This material is based upon work supported in part by Solvay S.A., by the STC Program of the National Science Foundation under Agreement No. DMR-0120967, and by the Office of Naval Research.

[1] B. Comiskey, J. D. Albert, H. Yoshizawa, and J. Jacobson, Nature (London) **394**, 253 (1998).
[2] A. Dodabalapur, Z. Bao, A. Makhija, J. G. Laquindanum, V. R. Raju, Y. Feng, H. E. Katz, and J. Rogers, Appl. Phys. Lett. **73**, 142 (1998).
[3] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, Appl. Phys. Lett. **82**, 3964 (2003).
[4] H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid, and C. Dehm IEEE Trans. Electron Devices **52**, 618 (2005).
[5] X.-H. Zhang, W. J. Potscavage, Jr., S. Choi, and B. Kippelen, Appl. Phys. Lett. **94**, 043312 (2009).
[6] T. D. Anthopoulos, B. Singh, N. Marjanovic, N. S. Sariciftci, A. M. Ramil, H. Sitter, M. Colle, and D. M. de Leeuw, Appl. Phys. Lett. **89**, 213504 (2006).
[7] N. Stingelin-Stutzmann, E. Smits, H. Wondergem, C. Tanase, P. Blom, P. Smith, and D. de Leeuw, Nature Mater. **4**, 601 (2005).
[8] I. McCulloch, M. Heeney, C. Bailey, K. Genivicius, I. MacDonald, M. Shkunov, D. Sparrowe, S. Tierney, R. Wagner, W. Zhang, M. L. Chabinyc, R. J. Kline, M. D. McGehee, and M. F. Toney, Nature Mater. **5**, 328 (2006).
[9] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dotz, M. Kastler, and A. Facchetti, Nature (London) **457**, 679 (2009).
[10] R. A. Street and A. Salleo, Appl. Phys. Lett. **81**, 2887 (2002).
[11] P. V. Pesavento, K. P. Puntambekar, C. D. Frisbie, J. C. McKeen, and P. P. Ruden, J. Appl. Phys. **99**, 094504 (2006).
[12] H. Klauk, U. Zschieschang, and M. Halik, J. Appl. Phys. **102**, 074514 (2007).
[13] C. Reese and Z. Bao, Adv. Funct. Mater. **19**, 763 (2009).
[14] T. D. Anthopoulos, F. B. Kooistra, H. J. Wondergem, D. Kronholm, J. C. Hummelen, and D. M. de Leeuw, Adv. Mater. (Weinheim, Ger.) **18**, 1679 (2006).
[15] M. Chikamatsu, S. Nagamatsu, Y. Yoshida, K. Saito, K. Yase, and K. Kikuchi, Appl. Phys. Lett. **87**, 203504 (2005).
[16] S. P. Tiwari, E. B. Namdas, V. R. Rao, D. Fichou, and S. G. Mhaisalkar, IEEE Electron Device Lett. **28**, 880 (2007).
[17] T. B. Singh, N. Marjanovic, P. Stadler, M. Auinger, G. J. Matt, S. Günes, N. S. Sariciftci, R. Schwödiauer, and S. Bauer, J. Appl. Phys. **97**, 083714 (2005).
[18] P. H. Wobkenberg, D. D. C. Bradley, D. Kronholm, J. C. Hummelen, D. M. de Leeuw, M. Colle, and T. D. Anthopoulos, Synth. Met. **158**, 468 (2008).
[19] E. von Hauff, J. Parisi, and V. Dyakonov, J. Appl. Phys. **100**, 073713 (2006).
[20] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C. W. Ou, P. K. H. Ho, H. Sirringhaus, and R. H. Friend, Nature (London) **434**, 194 (2005).
[21] M.-H. Yoon, C. Kim, A. Facchetti, and T. J. Marks, J. Am. Chem. Soc. **128**, 12851 (2006).
[22] A. Rolland, J. Richard, J. P. Kleider, and D. Mencaraglia, Jpn. J. Appl. Phys., Part 1 **35**, 4257 (1996).
[23] J. Zaumseil, K. W. Baldwin, and J. A. Rogers, J. Appl. Phys. **93**, 6117 (2003).
[24] E. J. Meijer, G. H. Gelinck, E. van Veenendaal, B.-H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, Appl. Phys. Lett. **82**, 4576 (2003).
[25] Z. Bao and J. Locklin, *Organic Field-Effect Transistors* (CRC, Boca Raton, 2007).
[26] E. J. Meijer, D. M. De Leeuw, S. Setayesh, E. Van Veenendaal, B. H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, and T. M. Klapwijk, Nature Mater. **2**, 678 (2003).
[27] F. R. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286 (1993).
[28] G. Gu, M. G. Kane, and S. C. Mau, J. Appl. Phys. **101**, 014504 (2007).
[29] U. Zschieschang, R. T. Weitz, K. Kern, and H. Klauk, Appl. Phys. A: Mater. Sci. Process. **95**, 139 (2009).
[30] C. C. Shih, Y. S. Lee, K. L. Fang, C. H. Chen, and F. Y. Gan, IEEE Trans. Device Mater. Reliab. **7**, 347 (2007).
[31] S. C. Deane, R. B. Wehrspohn, and M. J. Powell, Phys. Rev. B **58**, 12625 (1998).
[32] S. G. J. Mathijssen, M. Colle, H. Gomes, E. C. P. Smits, B. de Boer, I. McCulloch, P. A. Bobbert, and D. M. de Leeuw, Adv. Mater. (Weinheim, Ger.) **19**, 2785 (2007).
[33] X.-H. Zhang, S. P. Tiwari, and B. Kippelen, Org. Electron **10**, 1133 (2009).

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 128.193.164.203 On: Sun, 21 Dec 2014 07:41:09