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Pattern generation on silicon surfaces and $YBa_2Cu_3O_x$ thin films by a scanning tunneling microscope

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In this article, recent results employing scanning tunneling microscopy-based techniques for the generation of nanometer-scale patterns on hydrofluoric acid treated silicon(100) and $YBa_2Cu_3O_x$ superconducting thin films are presented. Furthermore, we were able to extract silicon (Si) atoms from Si(100)-1×1 surfaces, thereby producing silicon vacancies in the surface. These results thus demonstrate a possible approach for the construction of an atomic scale data memory as well as fabrication of artificial nucleation sites. The emission mechanism is believed to be field assisted evaporation due to the close proximity of the surface and the probe of the microscope.© *1995 American Institute of Physics.*

I. INTRODUCTION

Within the last several years, there has been great interest in the physics of mesoscopic (the range between atomic and micrometer size) devices and structures. Several very interesting phenomena such as the Aharonov–Bohm effect and universal conductance fluctuations have been seen in these devices, and possibly, many more interesting properties remain to be discovered. In order to build such devices to study some of these effects, it is necessary to have techniques capable of fabricating structures of nanometer dimensions.

In nanofabrication, long-term goals are

(i) to build the maximum number of device structures in a minimum space,
(ii) to keep these structures active after extensive use, and
(iii) to operate these structures in air environment.

The scanning tunneling microscopy (STM) has opened fascinating possibilities towards the miniaturization of electronic devices,[1] and single atom manipulations.[2,3]

Present commercial techniques used to modify solid surfaces work mostly in the micrometer range. However, there is a big effort to reach the nanometer range. This will offer new possibilities for mass storage, for submicron electronic devices, and for studying physical properties of specific nanolattices.[4] Although STM is well known as a technique to gain information about the surface of solids with atomic resolution,[5] only a few authors have investigated surface modifications by using STM.[6–10] When operated in the field emission mode it can generate an intense submicron beam of low-energy electrons. Because of absence of space charge and lens aberrations, the STM can produce a submicron beam even of few hundred volts with currents much higher than that are possible using more conventional techniques. Therefore, efforts in our laboratory have also been concentrated in developing scanning tunneling effect processing (STEP), in which tunneling electrons, ions, and/or atoms generated by a STM are used for nanometer scale fabrication.

In this article, our recent results employing STM-based techniques for the generation of nanometer-scale patterns on hydrofluoric acid (HF) treated silicon surfaces and high-temperature superconductor (HTSC) $YBa_2Cu_3O_x$ (YBCO) thin films are presented. The emphasis here is on process-oriented, rather than instrument-oriented issues. Thus, we restrict our discussion of STM-based modification techniques to processes, which lead to the creation of nanostructures. A significant feature of the present work is the demonstration that a localized change can be confined to a depth of a few nanometers below the surface.

II. EXPERIMENT

YBCO thin films were deposited on MgO and $SrTiO_3$ (100) oriented substrates by off-axis radio frequency (rf) magnetron sputtering from a stoichiometric composite target. The substrate temperature was varied between 700 and 800 °C. The total gas pressure ($Ar+O_2$) was 30 mTorr, with an oxygen partial pressure of 10 mTorr, and an rf power varying from 300 to 400 W. *P*-type, Si(100) wafers of 4–6 Ω cm were chemically cleaned by the RCA method[11] to remove the contaminants on the surface of the wafer and then rinsed with de-ionized (DI) water for 10 min. After this, a thermal oxide of 15 nm thickness was grown on the surface. The specimen (1×1 cm^2) was cut from the oxidized wafers. The samples were subsequently degreased using trichloroethylene, acetone, DI water, and then etched by dipping in dilute HF (10%–20%) for removal of oxide until the surface became hydrophobic. These were not rinsed again in DI water, but directly dried by blowing dry nitrogen gas to obtain hydrogen-terminated, chemically stable surfaces.[12,13]

In this study, a commercial STM (NanoScope II, Digital Instruments Inc.) was used as an electron source for nanofabrication as well as a microscope for imaging by changing bias voltage (V_b), tunneling current (I_t), and duration of current. The tunneling probe tips employed here were mechanically cut Pt-Ir (80:20). The tip condition was found to play a critical role in the process. All the images were taken in the constant height mode in air at room temperature.

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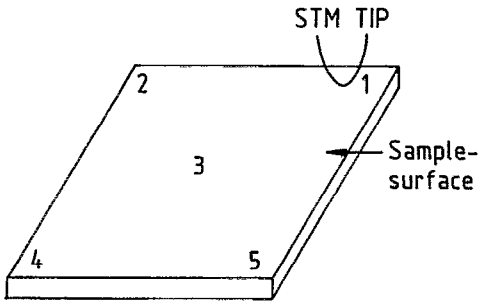
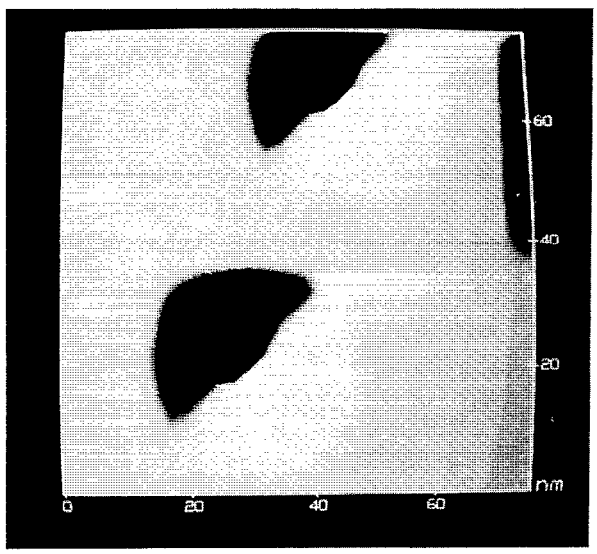


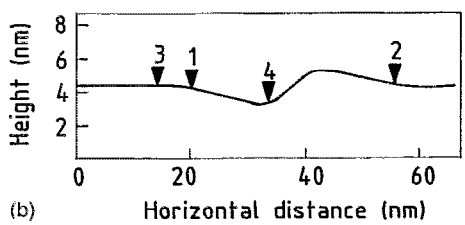
FIG. 1. Schematic drawing of the positioning of the STM tip for producing the nanometer structures.

III. RESULTS AND DISCUSSION

Figure 1 schematically shows the positioning of the tunneling tip to produce the nanometer structures on silicon or YBCO surfaces. We start with the tip at position 1 where we want to produce the first structure. After positioning the tip the bias voltage is slowly increased to about −3 V which results in increase in tip-to-sample distance. Then we increase the tunneling current to about 5 nA. This current, injected into a tiny region of the sample surface, leads to a significant temperature rise and to an electric field induced modification of the surface. As a result a pattern of nanometeric dimension is created in the sample surface. The current is then lowered to 1 nA in ~10 s and bias voltage is then reduced to about 1 V. We move the tip in the constant current mode to position 2 where we produce the second structure in the same way. Similarly, we generate structures at other locations on the surface as shown in Fig. 1.

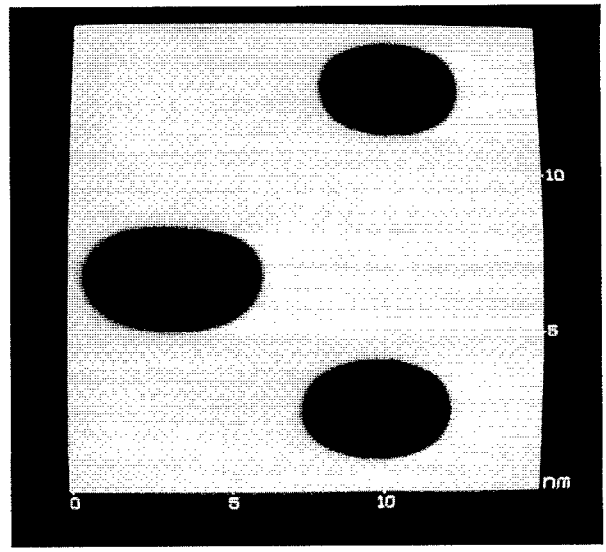


(a)



(b)

FIG. 2. (a) Surface modification on HF treated, p-Si(100), using a STM in air. Features were written using $V_{bias}=-3.2$ V and imaged at 1.2 V, $I_t=0.2$ nA with a 4.62 Hz scan rate. Dimensions of the features are approximately 35 nm×35 nm. (b) The cross-section through the hole is shown in the line trace. Cursor 1 and 2 indicates the width of the etched hole while 3 and 4 shows its depth.



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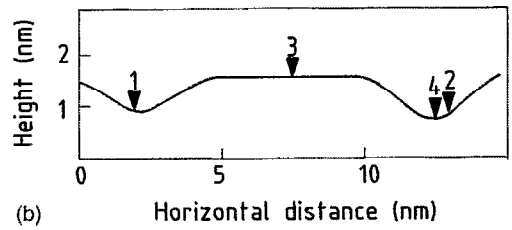
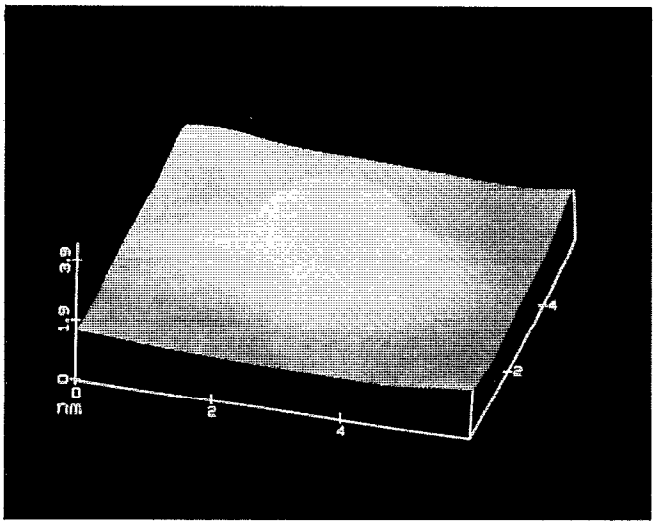


(b)

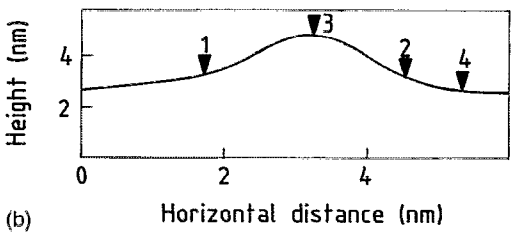
FIG. 3. (a) STM image of elliptical cavities produced in YBCO thin films in air. These cavities were written at $V_{bias}=-2.8$ V and $I_t=4.5$ nA at an interval of 10 nm. These were imaged at $V_{bias}=400$ mV and $I_t=0.2$ nA. (b) linear profile of section through the etched cavity hole in (a). The diameter of these cavities varies from 2–4 nm and the depth is 0.82 nm. Cursor 1 and 2 shows the distance between two cavities while 3 and 4 its depth.

Using the above procedure we generated two patterns in an HF treated silicon surface as shown in Fig. 2(a). These features were written with a $V_{bias}=-3.2$ V (sample negative) and imaged at 1.2 V. Under high current and high-voltage conditions, STM scans on these samples lead to significant modification of the surface region. The features created consist of shallow holes, a few angstroms deep, surrounded partially by hillocks. Figure 2(b) depicts the cross-sectional profile of the generated patterns of dimensions about 35 nm×35 nm×1 nm. These structures were created at an interval of 20 nm. Occurrence of hillocks at the corner in the etched hole may be attributed to some tip instability after the repeated transfer of material during hole formation. This suggests that tip shape plays a crucial role in surface modification by STM.

Figure 3(a) shows the patterns generated in YBCO films. These features were produced at $V_{bias}=-2.8$ V and tunneling current of about 4.5 nA. The three structures which are elliptical in shape are clearly visible as three cavities with a



(a)



(b)

FIG. 4. (a) STM image of a deposit made by a STM tip on a silicon surface. The diameter of the deposit is ≈2.82 nm, and was made with a tip bias of 3.5 V. (b) linear profile of section across the deposit. Its diameter is indicated by cursor 1 and 2 while 3 and 4 shows its height.

diameter of about 2–4 nm and are created at an interval of about 10 nm as seen in cross-sectional profile in Fig. 3(b).

Figure 4(a) depicts an image of a deposit made on a silicon surface with an STM tip at a bias voltage of 3.5 V (sample positive). The line profile across the deposit is shown in Fig. 4(b). Its diameter is ≈2.82 nm^2 and the individual atoms in the deposit are not resolved. We believe that the deposit is composed of clusters of atoms. It is essential to make a material analysis of the deposit to determine its nature. However, the structure is too small for conventional analysis such as Auger electron spectroscopy. But with the STM itself, we obtained current-voltage (I-V) characteristics with the STM tip located right above the deposit which is shown in Fig. 5 as curve a. The curve b in the Fig. 5 shows I-V characteristics of unmodified region of the silicon surface. The difference in I-V behavior revealed by these curves clearly shows that a modification of the surface has occurred and that the deposit is indeed not silicon. In fact, the linear dependence of the tunneling current on the biasing voltage shown in the I-V curve a, of the deposit indicates the metallic nature of the deposit. The metallicity of the deposit reveals that the atoms are deposited from the tip on the sample surface, probably through a field emission mechanism.

Further, using the technique of STM, we have successfully extracted single silicon atoms from predetermined positions on a silicon surface. This will be very useful to fabricate atomic-scale memory devices to store huge amounts of data on the surface by using a single silicon atom vacancy as

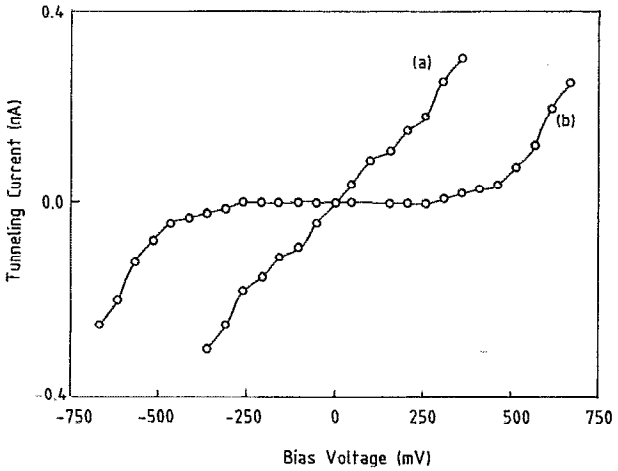


FIG. 5. I/V curves corresponding to Fig. 4(a). (a) is taken over the deposited region and (b) is obtained over the nonmodified region.

one bit of information. For this purpose we placed the well cleaned Pt-Ir tip at ≈5–6 Å above the silicon surface and applied a bias voltage between −3 and −5 V to the sample for 4–6 s. The vacancies created by extracting silicon atoms are indicated by an arrow in Fig. 6. This process was reproducible in about 50%–70% of the attempts. Using this approach, we can create unique atomic-scale structures by sequentially extracting single silicon atoms from predetermined positions.

Following the successful deposition of mould on silicon by Pt-Ir tip, we attempted to deposit some soft metals on silicon. With this aim we used mechanically cut aluminium tips for writing on silicon surfaces. Figure 7(a) denotes a view of aluminium metal lines drawn on a silicon surface. The grey scale image (brighter regions are higher) of the lines was obtained in the constant height mode with a bias voltage of 1.2 V (tip negative) and I_t=0.2 nA, and a scan

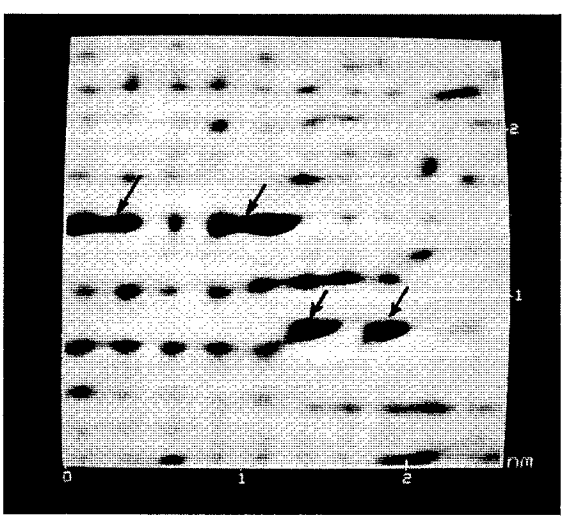
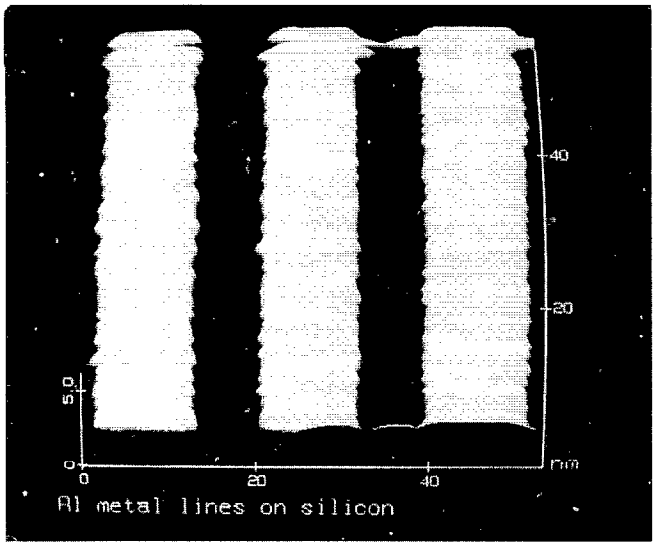
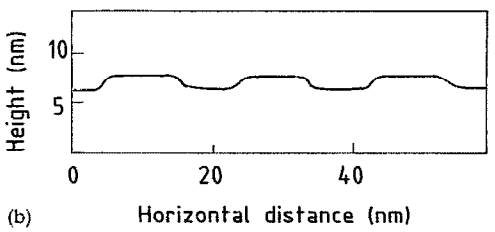


FIG. 6. STM image (2.5 nm×2.5 nm) showing the extraction of single silicon atoms from the Si(100) surface using a Pt-Ir tip. This image was taken at a sample voltage of 1.1 V and a tunneling current of 0.5 nA. Arrows indicates the regions from which atoms are extracted.



(a)



(b)

FIG. 7. (a) STM image of aluminium lines written at $V_{bias}=3.5$ V and $I_t=2$ nA. Aluminium tips were used for writing these lines. The width and height of these lines are nearly 10 and 1.5 nm, respectively. These parallel spaced lines were written at an interval of 6–8 nm. (b) Line profile across the lines taken along one direction.

rate of 8.62 Hz. These patterns consist of a series of parallel spaced lines. These lines were written at an $V_b=3.5$ V and $I_t=2$ nA. The average height and width of the written features is about 1.5 and 10 nm, respectively. The features were written at an interval of about 6–8 nm. The line profile across the lines is shown in Fig. 7(b). Scanning tunneling spectroscopy (STS) measurements revealed the metallic nature of these lines.

Once the atoms are transferred to the tip, we speculate that they are desorbed by the field. However, two other alternatives are also possible;

(i) Either they deposited on the surface but far from the region where the manipulation took place or
(ii) they become part of the tip.

If this is the case, it probably should not be at the apex. However the performance of the tip after surface modification did not show any deterioration indicating no deposit on apex of the tip.

From the above discussions, three interesting results arise. First, all the cavities or moulds are almost identical. This reveals the reproducibility of this method. Second, if one silicon atom vacancy can act as one bit of information, then this method has a potential for high-density data storage. Clearly at present it is not practical to utilize this procedure for data storage because of the low writing rate. The obvious next step should be to increase the rate for storing the information. Third, the performance of the tip does not seem to be affected by the writing process.

There are three possible mechanism for producing these surface modifications,

(i) mechanical interaction between tip and sample (indentation),
(ii) a process activated by the current, and
(iii) field-induced evaporation.

In our images, features are almost identical in shape/size. Thus, mechanical interaction between the tip and sample is completely ruled out. Since images can be obtained even when operating the STM in the constant current mode at 10 nA and low bias voltages (a few tens of mV); thus, we conclude from this that the current is not only the relevant parameter for producing these structures. In our laboratory, we have accumulated much data that suggest field-induced evaporation, i.e., the process of the removal of atoms from the surface under the action of high electric field[14] as the dominant mechanism for producing these nanostructures. Therefore, we strongly believe that high current, high voltage, hence high field, is necessary for surface modification by STM. A field evaporation mechanism may also explain some previously reported results on STM surface modification.[15–17]

IV. CONCLUSION

In conclusion, we have produced stable, low-voltage, nanometer-scale structures on dilute HF acid treated silicon surfaces and YBCO thin films using a STM in air. We consider field enhanced evaporation being a likely case for the generation of the observed structures. The technique allows writing and subsequent imaging of these time-stable structures with the same tip. We have demonstrated the possibility of extraction of a single atom from silicon surface. This could be of interest for the investigation of mechanical properties on a nanometer scale and for potential technological applications such as information storage devices and the production of devices on a nearly atomic scale. We believe that this opens new possibilities for the fabrication of nanostructures operative in air at room temperature.

[1] I. W. Lyo and P. Avouris, Science **245**, 1369 (1989).
[2] D. M. Eigler and E. K. Schwizer, Nature **344**, 524 (1990).
[3] R. S. Becker, J. A. Golovchenko, and B. S. Swartzentruber, Nature **325**, 419 (1987).
[4] R. E. Howard, P. F. Liao, W. J. Skocpol, L. D. Jackel, and H. G. Craighead, Science **221**, 117 (1983).
[5] G. Binnig and H. Rohrer, Phys. Rev. Lett. **49**, 57 (1982).
[6] M. Ringger, H. R. Hidber, R. Schlogl, P. Oelhafen, and H. J. Guntherodt, Appl. Phys. Lett. **46**, 833 (1985).
[7] M. A. McCord and R. F. W. Pease, J. Vac. Sci. Technol. B **3**, 198 (1985).
[8] M. A. McCord, D. P. Kern, and T. H. P. Chang, J. Vac. Sci. Technol. B **6**, 1877 (1988).
[9] C. R. K. Marrian and R. J. Colton, Appl. Phys. Lett. **56**, 755 (1990).
[10] E. J. Van Loenen, D. Dijkkamp, A. J. Hoeven, J. M. Lenssinck, and J. Dieleman, Appl. Phys. Lett. **55**, 1312 (1989).

[11] W. Kern and D. A. Puotinen, RCA Rev. **31**, 187 (1970).
[12] F. J. Grunthaner and P. J. Grunthaner, Mater. Sci. Rep. **1**, 69 (1986).
[13] T. Takahagi, I. Nagai, A. Ishitani, and H. Kuroda, J. Appl. Phys. **64**, 3516 (1988).
[14] E. W. Muller, Naturwissensehaften **29**, 533 (1941).
[15] D. W. Abraham, H. J. Mamin, E. Ganz, and J. Clarke, IBM J. Res. Dev. **30**, 492 (1986).
[16] H. J. Mamin, S. Chiang, H. Birk, P. H. Guethner, and D. Rugar, J. Vac. Sci. Technol. B **9**, 1398 (1991).
[17] J. A. Dagata, J. Schneir, H. H. Harary, C. J. Evans, M. T. Postek, and J. Bennett, Appl. Phys. Lett. **56**, 2001 (1990).