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Topical Review

Binary group III-nitride based heterostructures: band offsets and transport properties

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Abstract
In the last few years, there has been remarkable progress in the development of group III-nitride based materials because of their potential application in fabricating various optoelectronic devices such as light emitting diodes, laser diodes, tandem solar cells and field effect transistors. In order to realize these devices, growth of device quality heterostructures are required. One of the most interesting properties of a semiconductor heterostructure interface is its Schottky barrier height, which is a measure of the mismatch of the energy levels for the majority carriers across the heterojunction interface. Recently, the growth of non-polar III-nitrides has been an important subject due to its potential improvement on the efficiency of III-nitride-based opto-electronic devices. It is well known that the *c*-axis oriented optoelectronic devices are strongly affected by the intrinsic spontaneous and piezoelectric polarization fields, which results in the low electron–hole recombination efficiency. One of the useful approaches for eliminating the piezoelectric polarization effects is to fabricate nitride-based devices along non-polar and semi-polar directions. Heterostructures grown on these orientations are receiving a lot of focus due to enhanced behaviour. In the present review article discussion has been carried out on the growth of III-nitride binary alloys and properties of GaN/Si, InN/Si, polar InN/GaN, and nonpolar InN/GaN heterostructures followed by studies on band offsets of III-nitride semiconductor heterostructures using the x-ray photoelectron spectroscopy technique. Current transport mechanisms of these heterostructures are also discussed.

Keywords: III nitride heterostructures, non-polar nitrides, band offset engineering

(Some figures may appear in colour only in the online journal)

1. Introduction

1.1. Introduction to III-nitride heterostructures

Heterostructures are ubiquitous of semiconductor devices and most of semiconductor devices have two or more semiconductor materials. Heterostructures has brought tremendous changes in our everyday life and are heart for electronic and optoelectronic devices [1]. Heterostructures are used in different forms like diodes, transistors, thyristors, solar cells, detectors and laser diodes. A heterostructure is defined as a semiconductor structure in which the chemical composition changes with position [2]. The simplest heterostructure consists of a single heterojunction, which is an interface that occurs between two layers or regions of dissimilar crystalline semiconductors have unequal band gaps. From last two decade, III-nitride materials

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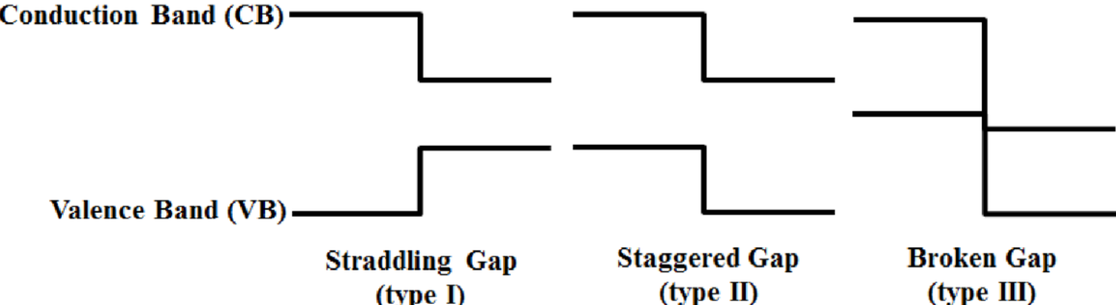

Figure 1. Three types of semiconductor heterojunctions.

are attracted to researcher due to its potential applications in light emitting diodes (LEDs), laser diodes (LDs), tandem solar cells and field effect transistors (FETs) [3–7]. In 1982, first GaN/AlN heterostructure were fabricated by Yoshida *et al* and demonstrated that the cathodoluminescence efficiency of the overlaying GaN has improved by using AlN buffer layer on Sapphire [8]. Later Akasaki [9] and Nakamura [10] have deployed the nucleation layer idea and have grown high quality GaN epitaxial layer by using a two-step growth, a low temperature buffer layer and high temperature GaN epitaxial layers. The achievement of p-type doping in GaN technology is another breakthrough in the history of III-nitride materials. Akasaki *et al* [11] reported low energy electron beam irradiation (LEEBI) converted an Mg-doped GaN layer to a p-type doped conductive layer. In 1993, first heterostructure based p-GaN/n-InGaN/n-GaN blue LEDs were fabricated by Nakamura [12] and he is awarded for Nobel Prize for this work in 2014. In 1996, Nakamura *et al* demonstrated first violet laser based on InGaN/GaN/AlGaN heterostructures [13]. The first breakthrough of AlGaN/GaN high mobility transistors based on heterostructure was demonstrated by Khan *et al* in 1994 [14].

In order to realize these devices, both growth of device quality epilayers and fabrication of heterojunctions (HJs) are required. One of the most interesting properties of a semiconductor heterostructure interface is its Schottky barrier height, which is a measure of the mismatch of the energy levels for the majority carriers across the interface. In the present review article, fabrication, determination of band offsets and effect on electrical transport properties are discussed.

1.2. Band offsets of semiconductor heterostructures

Two semiconductor materials of different band gap have discontinuities between the valence band maxima or conduction band minima at their interface, when both are joined. The discontinuities act as barriers to electrical transport across the interface. The semiconductor devices performance censoriously depends on valence band offsets (VBOs), conduction band offsets (CBOs) and interface quality in terms of roughness and absence of interface defects [15]. Based on the alignment of energy levels, heterostructures can be categorized in three classes; (i) type-I (straddling gap), (ii) type-II (staggered gap), and (iii) type -III (broken gap) [16]. Three types of band alignments are shown in figure 1. There are three significant material properties, which decide the type of heterostructure; band gap, electron affinity and work function. The electron affinity model (EAM) is first proposed model by which we can calculate band offsets of heterostructures in in an ideal case with assumption that no potential created at interface [17]. However, a deviation from the EAM model is generally observed as a change in the interface dipole. The band alignment between two semiconductors is controlled by the charge transfer across the interface and the resulting interface dipole in a fashion similar to Schottky barrier models [18]. Also many researchers have employed charge neutrality levels (CNL) to relate the relative contribution of the electron affinity model and the interface dipole in determining the band offsets [19]. The CNL concept was first formulated and used in studies of metal–semiconductor interfaces. CNL determines the barrier height at the interphase boundary, electronic properties of a bulk semiconductor saturated with intrinsic lattice defects, surface electronic properties, and limiting concentrations of shallow chemical impurities in semiconductors. This makes possible the use of the CNL to judge the electronic properties of defective nature semiconductors layers in hetero-epitaxy with various nucleation and strain relief layers and to construct the energy diagram of the interface. The band offset of heterostructures can be estimated by using x-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS) [20, 21]. At the interface of two semiconductors of different energy gaps, the offsets in the conduction and valence bands of heterostructure constituents accommodates the difference in the electronic properties between wide-gap semiconductor and narrow-gap semiconductor. Tailoring the band-offsets would leads to a new degree of freedom to tune the properties of the fabricated devices which uses the heterostructure. For example, the carrier injection and current transport and, in turn, the performance and reliability of heterojunction bipolar transistors (HBTs) and the carrier confinement in modulation doped field effective transistors (MODFETs) can be varied by the spike ΔE_c in the conduction band and step ΔE_v in the valence band at heterointerface [22].

1.3. Determination of band offsets at heterostructures using XPS

The band offsets have a large influence on the carrier transport across the junction and it is essential to measure the accurate value of CBO and VBO to understand the relationship

Table 1. Experimental band offset values from various previous reports.

Heterojunctions	VBO (eV)	CBO (eV)
InN/GaN	0.58 ± 0.08 [27], 0.85 [28],1.04 [29], 1.05 ± 0.25 [23]	2.22 ± 0.10 [27], 1.82 [28]
GaN/AlN	0.5 ± 0.1 [30], 0.70 ± 0.24 [23]	1.4 ± 0.1 [30]
a-plane GaN/AlN	1.33 ± 0.16 [31]	—
a-plane AlN/GaN	0.73 ± 0.16 [31]	—
InN/AlN	1.52 ± 0.17 [32], 1.81 ± 0.20 [23]	4.0 ± 0.2 [32]
AlN/GaN	1.36 ± 0.07 [33], 0.57 ± 0.22 [23]	—
AlN/InN	1.32 ± 0.14 [23]	—

between interface physical structure, electronic structure, and carrier transports. The VBO of two semiconductor materials can be determined from XPS measurements of the valence band and core-level photoemission from bulk like samples of the two constituent materials and a HJ sample forming the interface of interest. The over layer of this HJ sample must be sufficiently thin to allow XPS core levels from the underlying material to be probed due to the finite escape depth of the photoelectrons. The VBO is calculated from Kraut's method,

$$\Delta E_{\mathrm{v}} = (E_{\mathrm{CL1}}^{\mathrm{A/B}} - E_{\mathrm{CL2}}^{\mathrm{A/B}}) - (E_{\mathrm{CL1}}^{\mathrm{A}} - E_{\mathrm{VBM}}^{\mathrm{A}}) + (E_{\mathrm{CL2}}^{\mathrm{B}} - E_{\mathrm{VBM}}^{\mathrm{B}}), \quad (1)$$

where $(E_{\mathrm{CL1}}^{\mathrm{A/B}} - E_{\mathrm{CL2}}^{\mathrm{A/B}})$ is the energy difference between core level spectra of semiconductor A (CL1) and semiconductor B (CL2), which are measured in the HJ sample. $(E_{\mathrm{CL1}}^{\mathrm{A}} - E_{\mathrm{VBM}}^{\mathrm{A}})$ and $(E_{\mathrm{CL2}}^{\mathrm{B}} - E_{\mathrm{VBM}}^{\mathrm{B}})$ are the difference of core levels spectra and valance band maxima (VBM) of thick film of semiconductor A and bulk semiconductor B.

There are several studies are reported on the band offsets of III-Nitride heterostructures. Most earlier reports on this studies of III-Nitride semiconductors are inspiring for the recent studies. Martin [23, 24] *et al* reported on the basic and comprehensive studies of band offsets of III-nitride semiconductors. Ünlü *et al* [25] and Huai [26] reported on the theoretical studies of band offsets of the zinc-blende III-Nitride heterostrucutres. Experimental band offset values from wurtzite III-Nitride heterostrucutres from various previous reports are given in table 1. A part of this review will mostly focus on the band alignment studies of the InN/Si heterojuction, GaN/β-Si3N4 / Si (1 1 1) heterojunctions and InN/GaN heterojunctions.

1.4. Current transport mechanism of heterostructures

The mismatch of the energy levels for the majority carriers across the semiconductor heterostructures or metal/semiconductor interfaces can be explained in terms of Schottky barrier height (SBH). Metal–semiconductor contact is one of the most commonly used rectifying contacts. It is important to understand the nature of their electrical characteristics, in terms understanding the interface properties as well as forming robust Schottky diodes [34, 35].

Current–voltage (*I*–*V*) is one of the most widely used techniques to measure the SBH and forward bias *I*–*V* characteristics has often used to calculate the magnitude of the SBH [36]. Figure 2 shows the carrier transport mechanism in metal/semiconductor Schottky diodes. According to the thermionic emission (TE) theory, the carrier overcomes the neighbouring

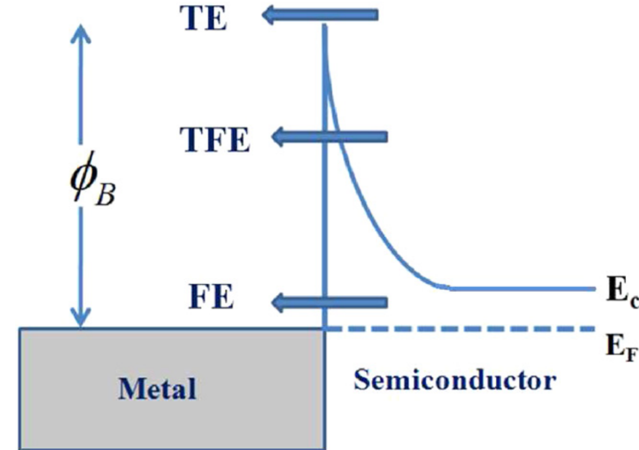

Figure 2. Different types of current transport mechanism in metal/semiconductor Schottky diodes.

energy barrier, with maximum barrier height above the Fermi level of metal region. The tunnelling of carriers at lower energies than the full barrier happens in heavily doped semiconductors. This mechanism is called thermionic field emission (TFE) and dominates significantly for semiconductors with high doping concentration (~1×10^{18} cm^{-3}). Field emission (FE) dominates in the metal/ semiconductor interface with large number of defect density. There are many reports on the fabrication and characterizations of metal/GaN Schottky diodes [37–40].

The most widely used techniques to measure the SBH and the ideality factor is the *I*–*V* technique, in which the forward bias portion of the *I*–*V* a characteristic is used. The transport of the charge carriers across the heterostructure interface is very sensitive to the magnitude of the SBH, hence the measurement of the SBH is interesting. The principal mechanism responsible for the current flow at the heterostructure based Schottky junction is the TE process. The values of SBH and the ideality factor for the junction are usually calculated by fitting a line in the linear region of the forward *I*–*V* curves using the TE model. According to the TE process [41], where $qV > 3kT$, the forward *I*–*V* characteristic of a Schottky diode is given by,

$$I = I_{\mathrm{s}} \exp\left(\frac{qV}{\eta kT}\right), \quad (2)$$

where

$$I_{\mathrm{s}} = AA * T^2 \exp\left(-\frac{\varphi_{\mathrm{b}}}{kT}\right), \quad (3)$$

here, I_s is the reverse saturation current, T is the measurement temperature, A^* is the Richardson's constant, k is the Boltzmann constant, q is the electron charge, φ_b is the SBH and η is the ideality factor. The TE model is valid when the transmission probability of the charge carriers across the junction is small.

In heavily doped semiconductors the barrier width at the junction decreases with doping of the carriers and hence the tunnelling probability for the charge carriers increases. The tunnelling of carriers at energies lower than the full barrier height can produce a current that is comparable or even more to the current generated by TE process. The tunnelling of the charge carriers effectively reduces the barrier for the thermionic emitted carriers by a specific amount, which depends on the width of the barrier and the temperature. The combined mechanism of partially thermally activation and the tunnelling is known as TFE. According to TFE model [42, 43], the forward I–V characteristic of a Schottky diode is given by

$$I = I_0 \exp\left(\frac{qV}{E_0}\right), \quad (4)$$

with,

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right) = \eta kT, \quad (5)$$

and,

$$I_0 = \frac{AA * T\sqrt{\pi E_{00}(\varphi_b - qV - V_n)}}{k \cosh\left(\frac{E_{00}}{kT}\right)} \exp\left[-\frac{V_n}{kT} - \frac{(\varphi_b - V_n)}{E_0}\right], \quad (6)$$

where, I_0 is the saturation current, T is the measurement temperature, A^* is the Richardson's constant, k is the Boltzmann constant, q is the electron charge, φ_b is the Schottky barrier height, η is the ideality factor and V_n is the energy difference between the conduction band minimum (E_c) and Fermi level (E_f) of the semiconductor and is given by $V_n = kT/q \ln(N_C/N_D)$, where N_C is the effective density of states in the conduction band and N_D is the carrier concentration of the semiconductor. The parameter E_{00} is the characteristic tunnelling energy that is related to the tunnel transmission probability and is given by

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_D}{m^* \varepsilon_s}\right)^{1/2}, \quad (7)$$

where m^* is the effective mass of the electron and ε_s is the dielectric constant of the semiconductor. The E_{00} parameter value determines whether the current conduction mechanism is by TE or TFE. According to the transport theory, TFE dominates only when $E_{00}/kT \approx 1$, because the Boltzmann distribution tail of thermionic emission drops off by a factor of $\exp(-1)$, which is much faster than the decrease rate of the tunnelling probability. On the other hand, TE is predominant when $E_{00}/kT \ll 1$ because the tunnelling probability drops off faster than TE [36].

Schottky diodes often exhibit temperature dependent barrier height and ideality factor evaluated from the I–V measurements, which is usually interpreted by the existence of barrier height inhomogeneities at the interface due to the several reasons like doping inhomogeneity, interface defects, bulk material defects, etc [44]. To explain the temperature dependent barrier height, Werner and Güttler [44] assumed the barrier heights are distributed according to a Gaussian type function which usually lead to an apparent barrier height that is temperature dependent. The total current is obtained by integrating the thermionic emission current with an individual barrier height and weighted by using the Gaussian distribution function.

2. Growth of III-nitride based heterostructures

2.1. GaN/Si heterostructures

GaN layers were grown on various substrates but Si is considered most promising candidate due to its availability in large wafer size with low cost, and having a well-known existing device technology [45]. In addition, the growth of GaN on Si allows good thermal management as Si has a better thermal conductivity than sapphire. However, due to large lattice mismatch (~17%) and thermal expansion coefficient mismatch (~56%) between GaN and Si, a large density of defects arising which rigorously affect the performance of devices [46]. Chu *et al* published first report of GaN growth on Si in 1971 [47]. To improve the interface quality, a thin interlayer of less mismatched materials can be used to passivate the defects and change the interface charge. Lei *et al* [48] reported zinc blende and wurtzitic GaN films on Si(1 0 0) by MBE, using a two-step growth process. However the lattice mismatch is higher on Si(1 0 0) than Si(1 1 1) and (1 1 1) orientation provides hexagonal lattice design, which is required for wurtzite GaN growth. In 1994, Stevens *et al* [49] reported wurtzite single crystalline GaN epilayers with 30 arcmin XRD FWHM, using a thin AlN buffer layer. The first LED on Si(1 1 1) was fabricated in 1997 by Guha *et al* [50] by using AlN buffer layers and the electroluminescence peak was centred in the ultraviolet around ~360 nm, with a full width at half maximum of ~17 nm. Up to date, various type of buffer layers were deployed, such as single or multi-AlN thin layers [51, 52], SiC [53], InGaN [54], AlN/GaN superlattice [55] and step-graded or composition-graded AlGaN/AlN [56] and Si_3N_4 [57].

2.2. InN/Si heterostructures

The achievement of high quality InN on Si has been delayed due to lack of suitable substrates, high In migration rate and relatively low decomposition temperature. Recently several studies have been reported on the growth of InN epilayers and nanostructures on, Si (1 1 1) [58, 59] and Si (1 0 0) [60] substrates. The Si substrates offer several advantages such as ease of cleaving, availability of conducting substrates in large size wafers at very low cost and suitability in device processing from the perspective of the devices. In our previous reports we have studied the growth and properties of InN epilayers by employing Si_3N_4 buffer layers on Si substrates

by plasma-assisted molecular beam epitaxy (PAMBE) [61]. Garcíaet *et al* reported on the growth of InN nanorods as well as compact layers on Si with AlN buffer layers [62]. In this review a brief discussion is carried out on the InN nanostructures as well as InN thin films grown on Si substrates.

InN nanostructures were directly grown on p-Si(1 0 0) substrates by nitrogen plasma-assisted molecular beam epitaxy system to fabricate InN/p-Si heterojunction. Two different types of nanostructures namely nano-dots (NDs) and nanorods (NRs) were grown by following two different growth conditions. The set of growth conditions includes, RF-plasma power was kept at 350 W, for NDs as well as for NRs. The fabrication of InN NDs consists of a two-step growth method. The initial low temperature buffer layer was deposited at 410 °C for 10 min. Further, the substrate temperature was raised to 500 °C to fabricate the nano-dots. The duration of ND growth was kept for 60 min. The growth temperature and duration of growth for NRs were kept at, 410 °C and 120 min, respectively. The nitrogen flow rate was maintained at 0.5 sccm and 1 sccm for the growth of NDs and NRs respectively. The beam equivalent pressure (BEP) of Indium was maintained at 2×10^{-7} mbar for NDs and the BEP was varied like 8.35×10^{-8} mbar, 1.45×10^{-7} mbar and 2.34×10^{-7} mbar for three samples of NRs. The structural characterizations of the as-grown nanostructures were carried out by field emission scanning electron microscopy (FESEM) and transmission electron microscopy (TEM). It could be observed that, the increase in the BEP of indium results in the increase in density of NRs. It is also observed that the height of NRs is increased with increasing the indium BEP. The dependence of the average height and density of the NRs on the indium BEP concluded. At the BEP of 2.34×10^{-7} mbar, the density of nanorods is approximately equal to 5.5×10^{-10} cm^{-2}, with an average height and diameter of 100 nm and 30 nm respectively. It is also observed that the nanorods grown with the BEP of 2.34×10^{-7} mbar are highly aligned. The NDs are vertically aligned and uniformly grown on the entire substrate. The average height and diameter of these dots were found to be 100 nm. As-grown NDs and NRs are fairly single crystalline, and are crystallized hexagonally along the [0 0 1] direction with uniform geometry. From the SEM and TEM results, the shape of the NDs corresponds to a perfect hexagon in the film plane and a truncated pyramid in the vertical direction with very clear crystallographic facets of hexagonal structure. It can be described more accurately as a truncated pyramid with hexagonal base with a base diameter few times larger than the height. Such growth behaviour is in agreement with that reported earlier [63].

InN films were grown on the Si (1 0 0) and Si (1 1 1) substrates by PAMBE. The substrates were chemically cleaned followed by dipping in 5% hydrofluoric acid to remove the surface native oxides. The substrates were thermally cleaned at 900 °C for an hour under ultra-high vacuum. Then the substrates were nitrided under the nitrogen plasma at the temperature of 700 °C. Then the low temperature buffer layers were grown at 400 °C of thickness 30 nm, followed by the high temperature films at 450 °C of thickness 250 nm. The nitrogen flow rate, RF-plasma powers were kept at 0.5 sccm, 350 W. The beam equivalent pressure of Indium was maintained at 2.1×10^{-7} mbar. The structural characterizations of the as grown films were carried out by high resolution x-ray diffraction (HRXRD) and SEM. The thin films grown on Si(1 0 0)and Si(1 1 1) surfaces exhibit the wurtzite crystal structure of the InN. The corresponding (0 0 0 2) XRD peak appears at 31.30 for InN. Nano sized grain distribution of the InN thin films grown on Si(1 0 0) as well as Si(1 1 1) are established from FESEM studies. While the films grown on Si(1 1 1) were densely packed, the films grown on Si(1 0 0) tended to be slightly porus. These behaviours might be due to the improved crystallinity of the Si_3N_4 intermediate layers in the case of Si (1 1 1).

2.3. InN/GaN heterostructures

The III-nitride based heterostructures have potential application in fabricating optoelectronic devices like LEDs, LDs and FETs. In order to realize these devices, both growth of device quality epilayers and fabrication of heterojunctions are required. High quality InGaN/GaN multi quantum well (MQW) grown by MBE have been reported by several groups. Shen *et al* reported 10-period of InGaN/GaN MQWs with different indium mole fractions [64]. Ng *et al* reported InGaN/GaN MQWs with abrupt interfaces between wells and barriers [65]. Che at al. reported 20 periods InN/InGaN MQWs using radio frequency PAMBE [66]. The InN/GaN heterostructure system has several advantages for the development of electronic devices operating in THz frequency range [67]. These advantages includes the high rate of optical phonon emission in InN (2.5×10^{13} s^{-1}), high peak value of the steady state electron drift velocity in InN (5×10^{7} cm s^{-1}) and large conduction band offset ensures the blocking of the conduction current over the barriers [67, 68].

However, the fabrication of high quality InN/GaN heterostructures is a challenging issue. The main reason is attributed to the difficulty in continuous growth of InN and GaN films because of large difference in the optimum growth temperature between them (InN ~500 °C and GaN ~750 °C). Further, this is also partly attributed to the difficulty in getting high quality InN epilayer at very low growth temperatures ~500 °C limited by the dissociation temperature of InN. In addition, the lattice mismatch between InN and GaN is as large as about 11% causing huge density defects at the interface. The interfacial structural defects of the heterostructures like InN/GaN, GaN/ZnO and GaN/AlN have been studied by several groups [69–71]. Yoshikawa *et al* [72] proposed and demonstrated the fabrication of InN/GaN MQWs consisting of 1 ML and fractional monolayer InN well insertion in GaN matrix. Che *et al* reported the fabrication of InN/GaN single-quantum well and double heterostructures by the radio-frequency PAMBE system [73]. We have grown InN/GaN heterostructures using PAMBE system. The InN films of 300 nm thick were grown epitaxially on 4 μm-GaN/Al_2O_3 (0 0 0 1) templates at different growth temperatures under nitrogen rich condition. The GaN templates were thermally cleaned at 700 °C for 5 min in the presence of nitrogen plasma. After thermal cleaning, the InN films were grown by using a two-step process: (a) growth of

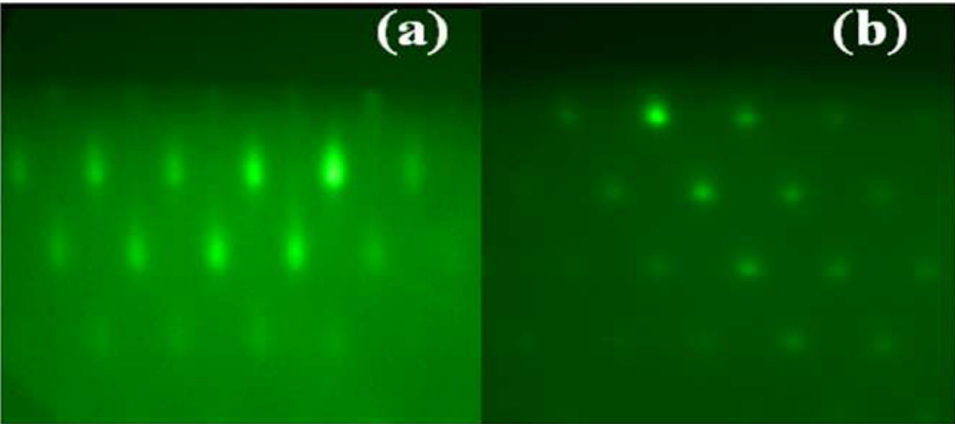

Figure 3. RHEED patterns of (a) *a*-plane (1 1 − 2 0) GaN and (b) *a*-plane (1 1 − 2 0) InN taken along (0 0 0 1) azimuth. Reprinted with permission from [88], copyright 2012 AIP Publishing LLC.

low temperature InN buffer layer of thickness 20 nm at 400 °C followed by, (b) the growth of high temperature InN epilayers. The range of high temperature growth were varied from 450–530 °C. The other detailed growth conditions can be found elsewhere [74]. After growth of InN/GaN heterostructures we have fabricated InN/GaN Schottky junctions and studied the temperature dependent electrical transport properties, which will be discussed on later section.

2.4. Nonpolar InN/GaN heterostructures

One of the useful approaches for eliminating the piezoelectric polarization effects is to fabricate nitride-based devices along non-polar and semi-polar directions. Growth of non-polar III-nitrides has been an important subject recently due to its potential improvement on the efficiency of III-nitride-based opto-electronic devices [75, 76]. However, growth of high quality InN is challenging due to its low thermal decomposition temperature and the high equilibrium vapour pressure of nitrogen. In last few years, considerable progress has been made in the growth of high-quality wurtzite InN by MBE and metal-organic chemical vapour deposition (MOCVD). Despite the study of non-polar GaN [77–79], there are very few reports on epitaxial growth of non-polar InN [80, 81]. The earlier reports on the InN on r-sapphire substrates indicate the growth of (0 0 1) cubic InN growth [82, 83] and polar (0 0 0 1) orientation [84]. The nonpolar *a*-plane InN was demonstrated by using GaN buffer layer on r-plane sapphire [85, 86]. In this section, MBE growth and properties of nonpolar InN on r-sapphire substrates with GaN buffer layer are discussed. The temperature growth of InN were varied from 470–530 °C. The other detailed growth conditions of InN/GaN heterostructures can be found elsewhere [86]. All the samples show the growth of nonpolar *a*-plane InN/GaN heterojunctions. The SEM and atomic force microscopy (AFM) studies show the rough surface of nonpolar *a*-plane InN on *a*-GaN /r-sapphire [86]. The RHEED patterns in the azimuths [0 0 0 1] for *a*-plane GaN and *a*-plane InN are shown in figures 3(a) and (b), respectively. The Bragg spots appear with weak streaky lines observed for *a*-plane GaN confirms the reasonable smooth surface [87]. The 3D growth of nonpolar *a*-plane InN is confirmed by spotty nature of *a*-plane InN [88].

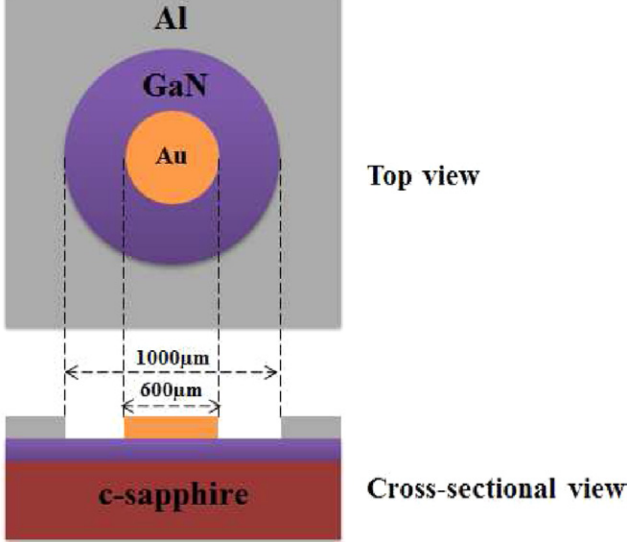

Figure 4. Schematic diagram of the metal/GaN Schottky diode.

2.5. Fabrication of Au/GaN heterostructures

In order to improve the performance of GaN based devices for optoelectronics and high temperature/high power electronics, it is necessary to develop more reliable and thermally stable Ohmic and Schottky contacts to this material. One of the most interesting properties of metal–semiconductor interface is its barrier height at the interface, which is a measure of the mismatch of the energy levels for the majority carriers across the interface. The barrier height controls the electronic transport across the interface and therefore, of vital importance to the successful operation of any semiconductor device. Several authors have found low experimental values of the barrier height compared to theoretical prediction and the ideality factor significantly larger than the unity. The low values of the barrier height result high leakage current, which is disadvantageous for the device performances. The experimental low value of the barrier height may be due to the enhanced

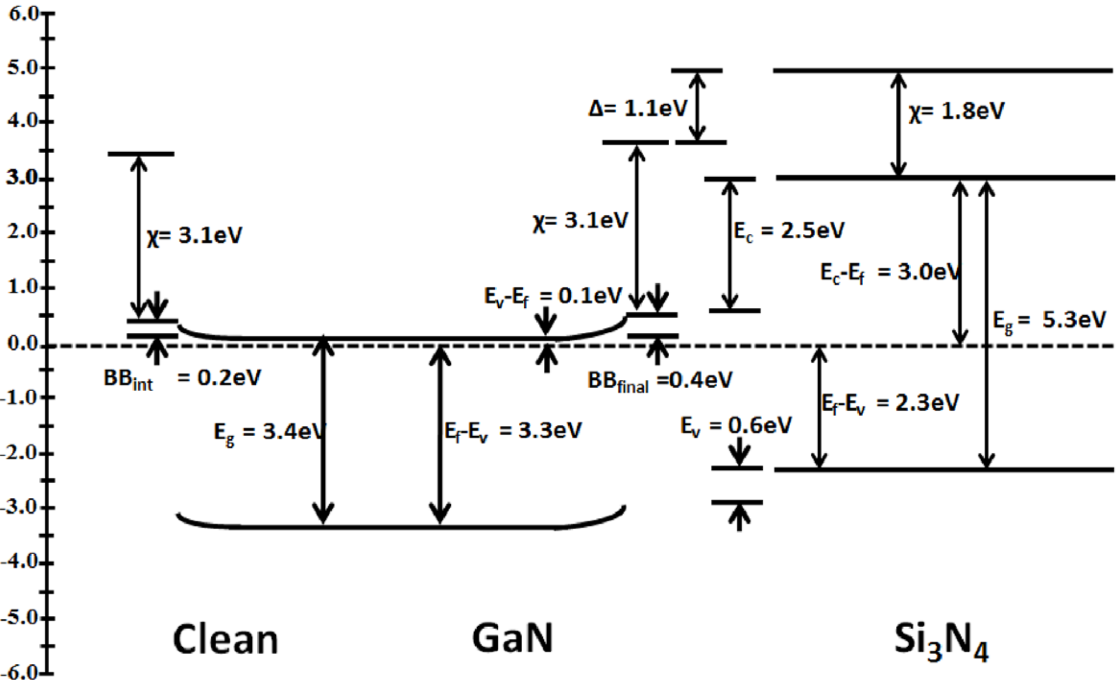

Figure 5. Bands deduced for the clean n-GaN surface and the interface between n-GaN and Si_3N_4. The valence band offset (E_v), conduction band offset (E_c), band bending (BB), and interface dipole (Δ) are presented. Reprinted with permission from [17], copyright 2003 AIP Publishing LLC.

tunnelling current through the metal–semiconductor Schottky barrier or the presence of charged surface states, metal induced gap states, bulk material defects, etc.

The schematic diagram of the Au/GaN Schottky diode is shown in the figure 4. Prior to the fabrication of Au/GaN Schottky diode, the GaN films were degreased in hot acetone and isopropyl alcohol for 5 min each, and etched in a solution of HF and H_2O (HF : H_2O = 1 : 10), rinsed with de-ionized water, and then dried with nitrogen gas. The inner circular Schottky contact of diameter 600 μm was made on GaN films by depositing Au (thickness ~200 nm) metal using RF-sputtering. The diameter of the inner circular metal dot was defined by the help of physical mask. Then, the outer circular Ohmic contact of diameter 1000 μm was made by thermally depositing Al (thickness ~200 nm) metal. The outer circular Ohmic contact was fabricated using standard photolithography process to pattern photo-resist for subsequent metallization and liftoff process. Finally, the device was annealed at 200 °C for 20 min in order to avoid the hydrogen influencing barrier height caused by RF sputtered metallization [89].

3. Band offsets of III-nitride based heterostructures by XPS

3.1. Band-alignment at GaN/β-Si3N4 /Si (1 1 1) interfaces

Silicon Nitrides (Si_3N_4) layers were used as gate dielectric in field-effect transistors (FETs), passivation layer in high voltage devices and buffer layers for GaN technology [90, 91]. Nakasaki *et al* [92] has grown Si_3N_4 on GaN by chemical vapour deposition and determined the valance band offset ΔE_v ~ 1.0–1.2 eV at Si_3N_4/GaN interface using XPS core level measurements. Cook *et al* [17] studied the band alignment between n- and p-type GaN and Si_3N_4 interfaces by XPS and UPS. The energy bands deduced for n-type GaN and Si_3N_4 are shown in figure 5. The VBO (ΔE_v), CBO (ΔE_c) and interface dipole (Δ) were determined 0.6 eV, 2.5 eV and 1.1 eV, respectively. For p-type GaN and Si_3N_4 were determined ΔE_v ~ 0.4 eV, ΔE_c ~ 2.3 eV and Δ ~ 1.0 eV and shown in figure 6. Lee *et al* [93] has grown ultrathin β-Si_3N_4 layer by N_2-plasma nitridation of Si(1 1 1) substrates at 900 °C and measured band offsets by photoelectron spectroscopy (PES) using synchrotron radiation. Figure 7 shows the valence-band PES spectrum and contains both the PES signals from the β-Si_3N_4 film and from the Si(1 1 1) substrate. The VBO and CBO values were determined as 1.8 eV and 2.4 eV, respectively. In our previous report [94], we have grown ultrathin films of β-Si_3N (0 0 0 1) on Si (1 1 1) surface by exposing the surface to radio- frequency nitrogen plasma with a high content of nitrogen atoms and using β-Si_3N_4 layer as a buffer layer, GaN epilayers were grown on Si (1 1 1) by plasma-assisted molecular beam epitaxy. The VBO and CBO were determined at of GaN/β-Si_3N_4 and β-Si_3N_4/Si heterojunctions by XPS and shown in figure 8. The VBO, CBO and interface dipole were measured ΔE_v ~ 1.84 eV, ΔE_c ~ 2.6 eV and ΔE_v ~ 0.46 eV, respectively at β-Si_3N_4/Si interface and ΔE_v ~ 0.41 eV, ΔE_c ~ 2.29 eV and ΔE_v ~ 1.29 eV, respectively at GaN/β-Si_3N_4 interface.

3.2. Band alignment at high-k gate oxide/GaN interface

Moore's prediction that the number of transistors per wafer would be doubled-up every 18–24 months has led to higher device density. As the transistor size decreases, the electric field increases, which required the materials that can sustain in high electric field [95]. GaN based high electron mobility transistors (HEMTs) have excessive demand in high power electronics

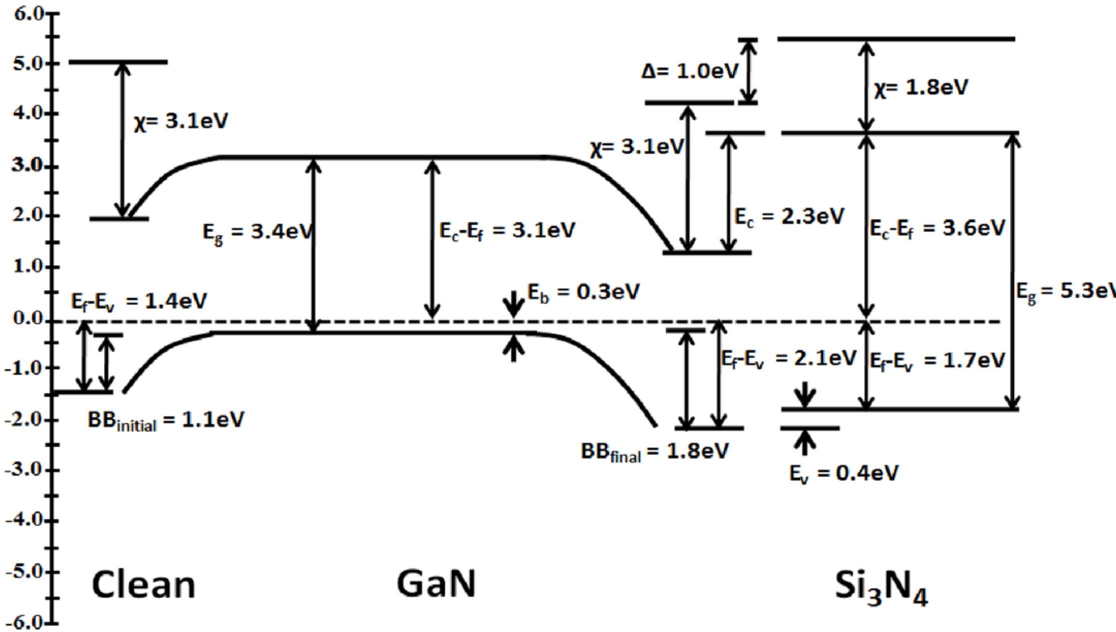

Figure 6. Bands deduced for the clean p-GaN surface and the interface between p-GaN and Si_3N_4. The valence band offset (E_v), conduction band offset (E_c), band bending (BB), and interface dipole (Δ) are presented. Reprinted with permission from [17], copyright 2003 AIP Publishing LLC.

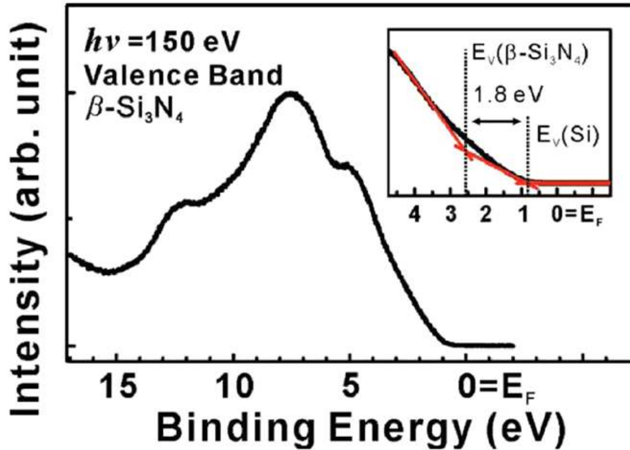

Figure 7. Valence-band spectrum of β-Si_3N_4/Si (1 1 1). Reprinted with permission from [93].

market because of their inherent high breakdown voltage, high two-dimensional electron gas (2DEG) concentration, and high saturation velocity [96]. However, device performances of AlGaN/GaN HEMTs are seriously limited by several drawbacks such as, drain-current collapse phenomenon, reduction of breakdown voltages, microwave power, and efficiency and increase the noise of the device [97]. To solve these problems, research community is optimizing the crystalline quality, interfaces and the surfaces, hence the electrical properties of the HEMT heterostructures. Along with this, significant research is going on metal-oxide-semiconductor high-electron mobility-transistors (MOS-HEMT). Up to date various type of gate dielectrics were used such as SiO_2 [98], Ga_2O_3 [99], Al_2O_3 [100], HfO_2 [101], Sc_2O_3 [102] and MgO [103]. The use of high-k dielectrics as a passivation layer on GaN-based high voltage devices and as a gate dielectric in FETs devices requires knowledge of the band alignment at high-k gate oxide/GaN interface. Cook *et al* [104] determined band alignment at HfO_2/GaN interface and studied the annealing effect. Figure 9 and 10 shows band offsets between n-type GaN and HfO_2 before and after annealing at 650 °C, respectively. The VBO and CBO were calculated ΔE_v ~ 0.1 eV and ΔE_c ~ 2.5eV before annealing and ΔE_v ~ 0.3 eV and ΔE_c ~ 2.3 eV after annealing of HfO_2/GaN heterojunctions. The interface represents type-II band alignment and the thermal stability of the HfO_2 film significantly affects the electronic properties at the GaN/HfO_2 interface. Chen *et al* [105] reported MgO epitaxial growth by RF plasma-assisted molecular beam epitaxy on top of thick GaN templates on sapphire substrates. The VBO and CBO of MgO/GaN heterojunctions were measured by XPS and shown in figure 11. The band gap difference of 4.36 eV between the MgO and GaN materials leads to band alignment ΔE_v ~ 1.06 eV and ΔE_c ~ 3.3 eV at MgO/GaN interface. The high band offsets provide the effective reduction of current collapse, a low interface state density with GaN and also well suited to high-temperature applications. The Sc_2O_3 has a bixbyite crystal structure, with a 9.2% lattice mismatch to GaN, a high dielectric constant (~14), a reasonable band gap (6.0 eV) and low trap densities which reduce the current collapse in AlGaN/GaN heterostructure transistors [106]. Chen *et al* [107] measured the energy discontinuity at Sc_2O_3/GaN heterostructures using XPS and shown in figure 12. A value of ΔE_v ~ 0.42 eV was obtained using the Ga 3d energy level as a reference and ΔE_c is 2.14 eV in Sc_2O_3/GaN system. An XPS core level measurement is a powerful tool to determine the band offsets between oxide and semiconductor heterostructures.

3.3. Band alignment at InN/Si interface

Since silicon is the most sought semiconductor material, it is very important to understand the band alignment of InN

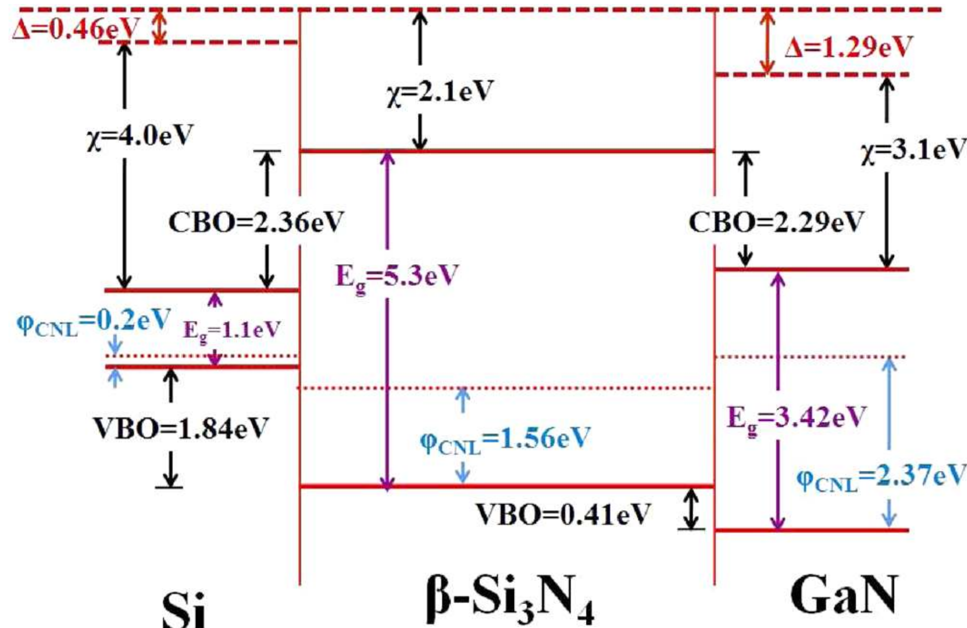

Figure 8. Schematic energy band diagram of GaN/β-Si3N4/Si interfaces as determined by XPS. The dashed line at the top corresponds to the electron affinity of the β-Si3N4 surface, which is common in both interfaces. The deviation from the electron affinity model is shown by Δ, and the charge neutrality level is indicated by a dotted line within the band gap. Reprinted with permission from [94], copyright 2012 Elsevier.

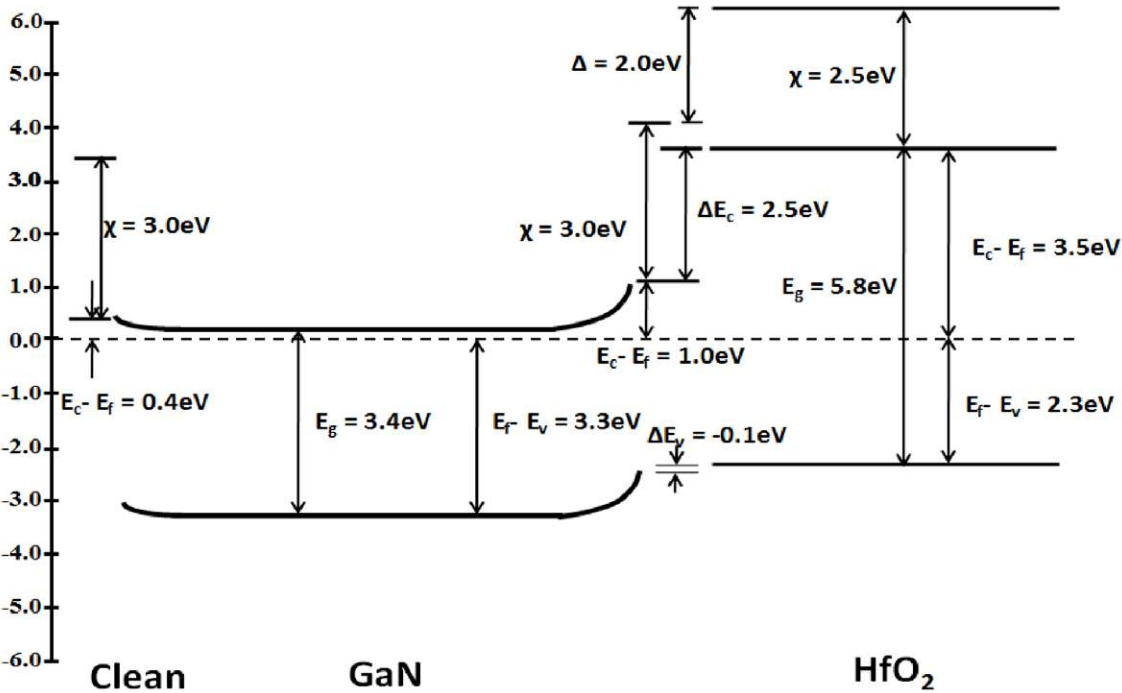

Figure 9. Deduced bands for the clean n-GaN surface and the interface between n-GaN and HfO_2 before annealing. The valence band offset (ΔE_v), conduction band offset (ΔE_c), band bending, and interface dipole (Δ) are represented. Reprinted with permission from [104], copyright 2003 AIP Publishing LLC.

based devices and their heterojunction behaviour prior to their adoption in the fabrication of optoelectronic devices. Our report [60] on the n-InN nano-dot/p-Si heterojunction established the band offset values by capacitance–voltage measurements. Our previous [108] study is evident on the determination of valence band and conduction band offsets of InN/p-Si heterojunction with well accepted InN band gap value of 0.65–0.8 eV by using XPS. We have used the method of CNLs [109] to cross check the band offset values which gave a reasonably good agreement with the experimental determinations.

The band offsets of InN/p-Si heterojunction were estimated by the results of XPS, obtained for a 200 nm InN film, cleaned Si substrate and 4 nm thin InN/p-Si heterojunction. The growth process of these films and details of band offset estimation can be found elsewhere [108]. Hence, the VBO value is calculated to be 1.39 ± 0.01 eV. The band gap values of 0.7 eV and 1.12 eV were considered for InN and Si,

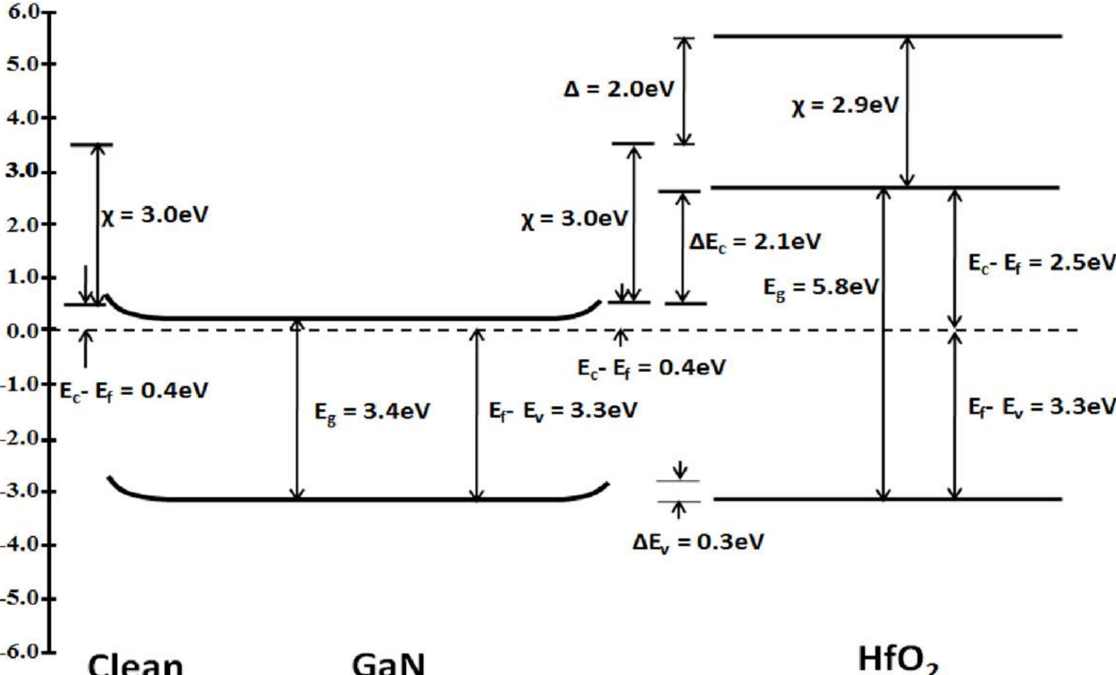

Figure 10. Deduced bands for the clean n-GaN surface and the interface between n-GaN and HfO_2 after annealing at 650 °C. The valence band offset (ΔE_v), conduction band offset (ΔE_c), band bending, and interface dipole (Δ) are represented. Reprinted with permission from [104], copyright 2003 AIP Publishing LLC.

respectively. ΔE_c was calculated to be 1.81 eV, and as a result, a type-III band alignment for the InN/p-Si heterojunction has been proposed, as shown in figure 13. The InN/p-Si band offsets of these results can be found significantly different from the band offset values reported by Yoshimoto *et al* [109], in particular for the CBO. A type-II band alignment for InN/p-Si heterojunction was reported by Yoshimoto *et al* This is attributed to the major difference in the band gap value of the InN, i.e. 0.7 eV which is considerably lesser than that of 1.8–2 eV considered by Yoshimoto *et al* [109].

The band offsets can also be determined by the relative position of the CNL of the two materials if the density of states is high or if the CNL of the two materials is similar in the relative energy. In the present case, we found that, the experimental results are in agreement with the CNL model within the experimental measurement error. A comparative interpretation of the experimentally derived and predicted from the CNL model band alignment with the band alignment obtained from EAM had been performed by constructing the band alignment diagram. Initially the diagram was aligned with respect to the vacuum level at Si by the electron affinity of χ_{Si} = 4.05 eV. The band gaps of both the material are indicated. Then the CBs and VBs are aligned by substituting the CBO and VBO values respectively, obtained from the experimental results or CNL model. Both the methods resulted in the reasonably matching of band offset values and no significant difference was observed in the band alignments. A deviation of 0.06 eV was observed between experimental results as well as the results from the CNL model. The EAM of heterojunction band alignment assumes that the vacuum levels would align at the interface so that conduction band minima of the materials would get aligned with respect to their electron affinities. Also, the basic assumption in the EAM is that the interface is formed without perturbation of the surface electronic states of either of the two materials. The observed difference between the prediction of the EAM and the experimentally observed band offset attributed to a change in the interface dipole [108].

3.4. Band alignment at InN/GaN interface

The band offsets have a large influence on the carrier transport across the interface and electron–hole pair recombination. It is very crucial to study conduction and valence band offsets between InN and GaN heterojunction from a fundamental point of view as well as fabricating optical and electronic devices. The present section focuses on the determination of band offsets at InN/GaN heterostructures. The earlier report on the VBO value of InN/GaN was found to be 1.05 ± 0.25 eV which was measured almost two decades ago [23]. Theoretically estimated the VBO at an InN/GaN heterojunction was found to be ΔE_v = 0.48 eV [26]. Wu *et al* [29] demonstrated the VBO calculation using photoelectron spectroscopy for In/Ga-polar and N-polar InN/GaN heterojunction. The determined VBO's are 1.04 and 0.54 eV for In/Ga-polar and N-polar InN/GaN heterojunction, respectively. These values may have large error as the VBOs were calculated using In 4d and Ga 3d peaks. King *et al* [27] demonstrated the accurate VBO measurement of InN/GaN heterojunction grown by MBE system and was found to be 0.58 eV and was calculated using In 3d and Ga 2p. Mahmood *et al* [28] estimated the VBO of InN/GaN heterojunction grown by MOCVD using internal photoemission spectroscopy and was found to be 0.85 eV. Figure 14 shows the room-temperature band alignment at an InN/GaN

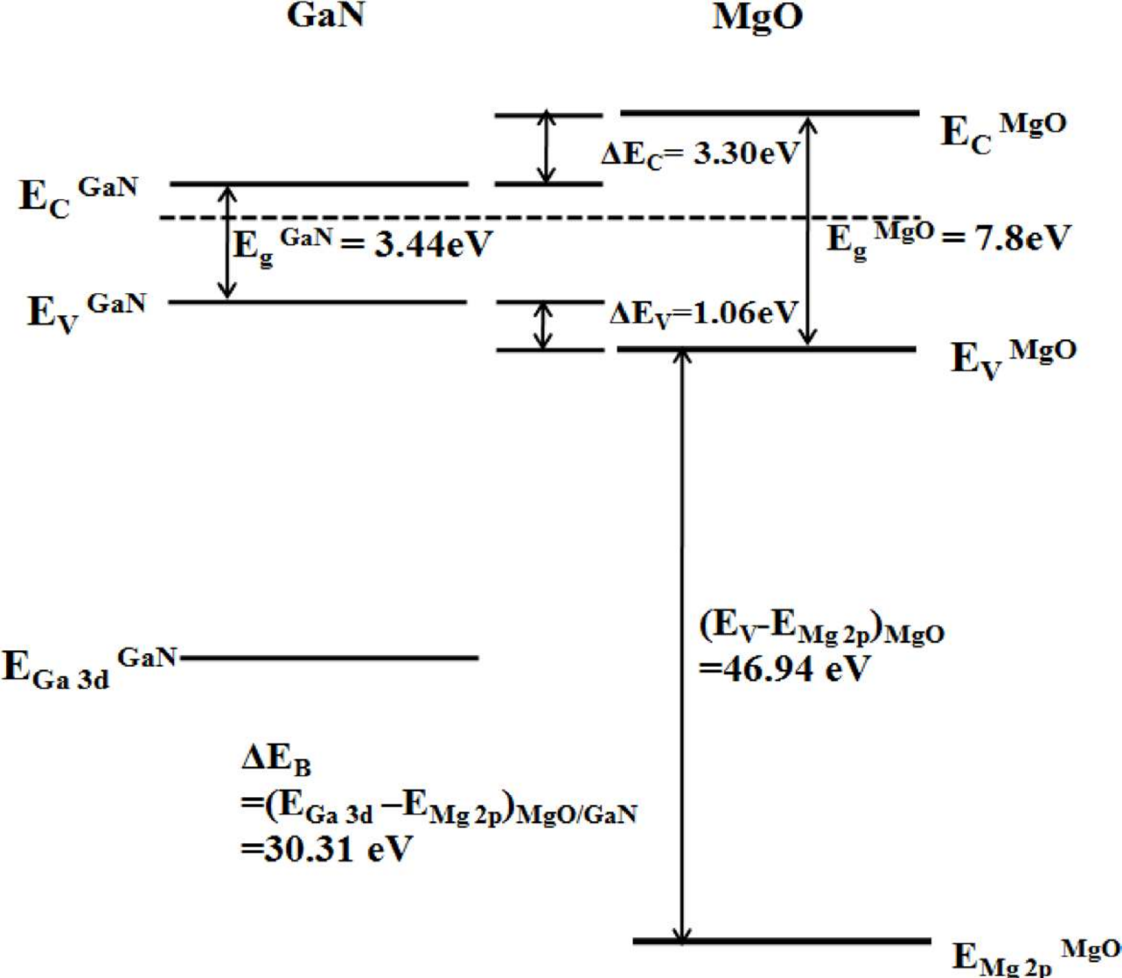

Figure 11. Energy band diagram of a thin MgO/GaN heterojunction interface as determined by XPS. Core level separation measured across the interface is represented by ΔEB. Reprinted with permission from [105], copyright 2006 AIP Publishing LLC.

heterojunction [27]. The heterojunctions form in the type-I straddling configuration.

3.5. Band alignment at non-polar nitride interface

In recent years, nonpolar nitride materials have drawn great interest due to absence of spontaneous polarization at the interfaces and its applications in high bright LEDs and normally-off HEMT devices. The spontaneous polarization affects the band alignment at the heterojunction and so far nonpolar band offsets have been studied by few. Li *et al* [110] reported the VBOs of wurtzite *c*-plane and *a*-plane AlN/GaN heterojunctions grown by MOCVD. The VBOs were found to be 0.82 ± 0.15 and 0.63 ± 0.15 eV for the *c*-plane and *a*-plane AlN/GaN heterojunctions, respectively. The discrepancy in VBOs of heterojunctions with different orientations could be due to the spontaneous polarization effect and the VBO of the *a*-plane AlN/GaN is closer to the intrinsic value due to absence of polarization effects. GaN and ZnO have the same crystal structure, close lattice parameters and thermal expansion coefficients. The polarization effects on band offsets can be studied by determining the band offsets at GaN/ZnO and InN/ZnO heterojunctions. Liu *et al* [111] studied the band offsets of polar and nonpolar GaN/ZnO heterostructures by synchrotron radiation photoemission spectroscopy. The samples were prepared by pulsed laser deposition techniques and the VBOs were found to be 0.7 ± 0.1 and 0.9 ± 0.1 eV for the polar (*c*-plane) and nonpolar (*m*-plane) GaN/ZnO heterojunctions, respectively. Yang *et al* [112] reported the VBOs of the wurtzite polar *c*-plane and nonpolar *a*-plane InN/ZnO heterojunctions grown by MOCVD. The VBOs are directly determined 1.76 ± 0.2 eV for polar and 2.20 ± 0.2 eV for nonpolar by XPS. The heterojunctions form in the type-I straddling configuration with a conduction band offsets of 0.84 ± 0.2 eV and 0.40 ± 0.2 eV. The difference of VBOs of polar and nonpolar structures is due to the large spontaneous and piezoelectric polarization effects and the discontinuity of polarizations across a heterojunction, which induce a fixed polarization charge at the interface.

4. Current transport studies of III-nitride heterostructures

4.1. Electrical transport properties of GaN/Si heterojunctions

There are few previous studies on the transport properties of GaN/Si heterojunctions [113–115]. In this review the transport mechanisms of GaN/Si heterojunctions are established by *I–V*

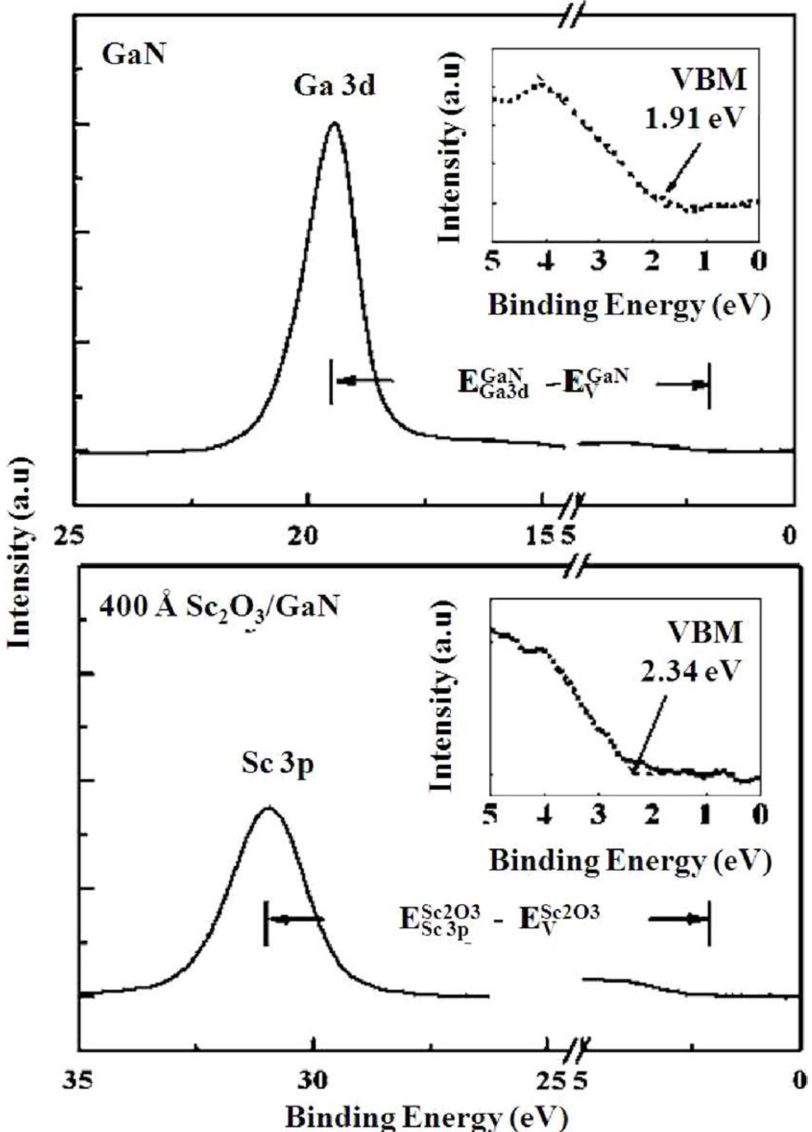

Figure 12. Energy band diagram of thin Sc_2O_3/GaN heterojunction interface. Reprinted with permission from [107], copyright 2006 AIP Publishing LLC.

characteristics obtained at room temperature. Room temperature I–V characteristics of the GaN/p-Si(1 0 0) heterojunctions were measured and the behaviour is shown in the figure 15. Three different samples were grown with various nitridation conditions such as, absence of substrate nitridation, nitridation at 600 °C and nitridation at 800 °C [113]. The diodes exhibit the turn on voltage of about 0.4 V but the allowing current at turn on voltage is strongly dependent on the nitridation conditions. The non-stoicheometric Si_xN_y layers present in the sample with low temperature substrate nitridation act as a thin insulator layer which reduces the current flow. Both the diodes show similar rectifying behaviour with the on/off ratio of ~11 at 3 V. But the diode with high temperature substrate nitridation exhibits a current of 10^{-6} A at the turn on voltage. It shows a noticeable reduction in the forward current, it exhibits the best rectifying behaviour with on/off ratio ~230 at 3 V. A considerable reduction in the leakage current is attributed to the low defect concentration or trap centres in the film and interfacial layers due the introduction of stoicheometric Si_3N_4 buffer layer.

The I–V curves of all the three diodes were analysed at low voltage regions (<0.5 V) by using the standard diode equation as given in equation (2). The diode grown with the absence of substrate nitridation exhibited highest ideality factor, η ~ 6 and the diode fabricated with low temperature substrate nitridation resulted in an ideality factor of ~4. The high ideality factors observed are often attributed to the presence of defect states which causes the deep level assisted tunnelling or lateral in homogeneities of the barrier height at the interfaces. Diode fabricated with high temperature substrate nitridation showed an ideality factor ~1.5. This behaviour shows transport is governed by the recombination at space charge region mechanism at low voltages. According to the TE model, the saturation current (I_s) is represented by equation (3), where A is the contact area of the junction, A^* is the Richardson constant which is 112 A cm^{-2} K^{-2} for n-Si [116], due to inverted rectification, and φ_b is the effective barrier height. φ_b is obtained to be 0.63, 0.71, 0.82 eV for the diodes grown with absence of nitridation, low temperature nitridation, and high temperature nitridation, respectively. Barrier

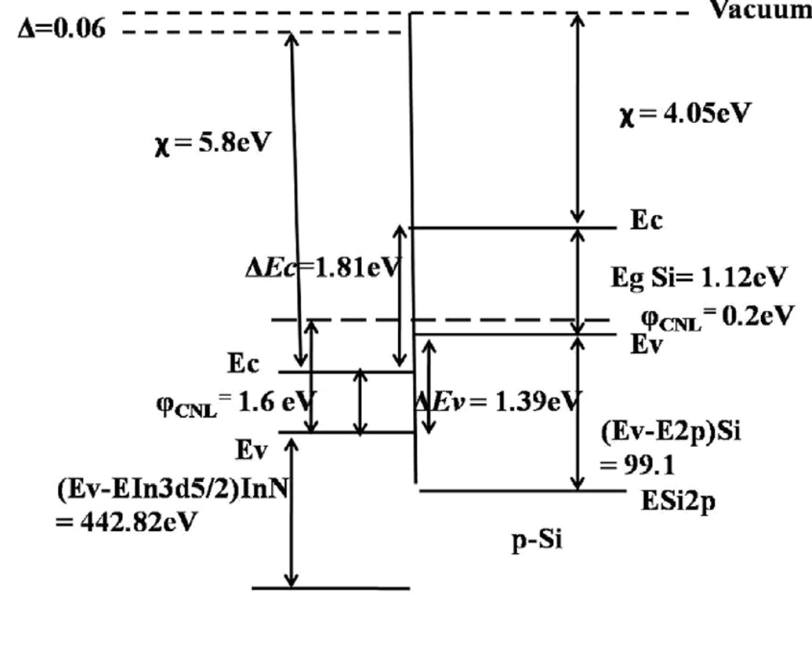

Figure 13. Schematic illustration of type-III band alignment of InN/p-Si. The top dashed line corresponds to the electron affinity of Si. The deviation in the band alignments from the electron affinity model is indicated by Δ. Reprinted with permission from [108], copyright 2011 AIP Publishing LLC.

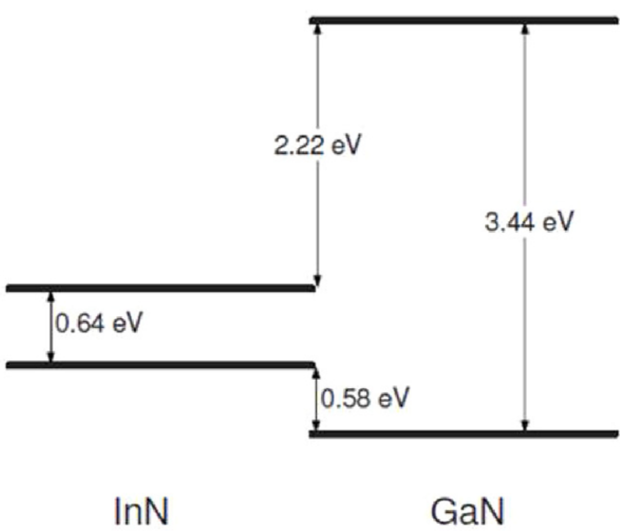

Figure 14. Schematic of the room-temperature interface band alignment at an InN/GaN heterojunction. Reproduced with permission from [27], copyright 2008 American Physical Society.

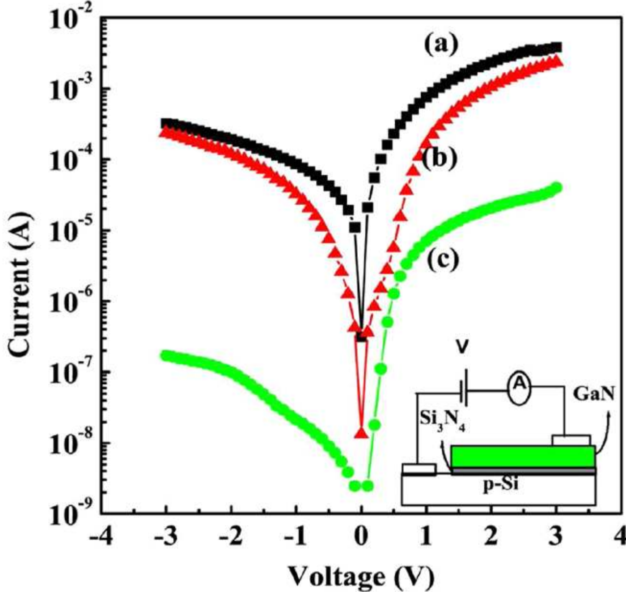

Figure 15. Room temperature *I–V* characteristics of the GaN/p-Si heterojunctions grown with (a) absence of nitridation, (b) nitridation at 600 °C and (c) nitridation at 800 °C. Reproduced with permission from [113], copyright 2011 AIP Publishing LLC.

height values confirm the tunnelling of carriers in the samples grown without nitridation as well as low temperature nitridation.

The transport characteristics of n-GaN/p-Si heterojunctions exhibit an interesting inverted rectification behaviour irrespective of nitridation conditions. A quantum well for electrons is formed on the p-Si side as shown in the band alignment diagram (figure 16). The Si is inverted in the interface with n-GaN. Here the smaller band gap material Si is comparable to the metal and the conduction band offset is equivalent to a Schottky barrier in an *n*-type diode. The barrier height obtained from the *I–V* characteristics is 0.82 eV, is in close agreement with the conduction band offset of GaN/Si heterojunction, i.e. 0.95 eV. The band alignment diagram of n-GaN/p-Si is shown in the figure 16 certainly renounces the possibility of inter-band tunnelling.

4.2. Carrier transport studies of InN/Si heterojunctions

InN is an important semiconductor material with superior electronic transport properties such as high mobility and

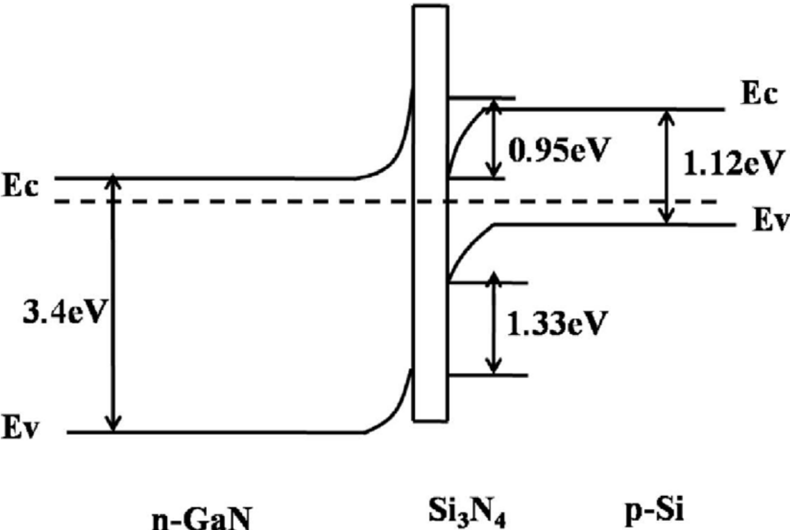

Figure 16. Energy band alignment diagram of the n-GaN/Si_xN_y/p-Si heterojunction under thermal equilibrium. Reproduced with permission from [113], copyright 2011 AIP Publishing LLC.

high saturation velocity at room temperature, which make it suitable for high-efficiency terahertz emitters, detectors, high-frequency electronic devices [117–119]. Device prototypes employing semiconductor nano-structures have already been interest of the research community. Electrical behaviour of nano-devices with nano-structures is critical to design and fabricate high performance electronic or optoelectronic devices. In comparison with the thin-film devices, transport behaviours through interfaces has been seen to differ in nature (e.g. tunnelling versus thermionic) as the lateral size of the contact is varied. Also, the reduction in the density of extended defects in the case of nano-structures offers several advantages in terms of lower leakage and recombination currents as compared to the thin-film counterparts, provided that surface recombination is suppressed [120].

Recently several studies have been reported on the electrical properties and transport mechanisms of InN/Si heterojunctions. We reported on the barrier inhomogeneity and electrical properties of InN nano-dots/Si(1 1 1) heterojunction diodes [121] and transport and infrared photoresponse properties of InN nanorods/Si heterojunction are studied and concluded that, InN NRs/Si heterojunction device can be used for IR detectors [122]. Wu *et al* observed the near-infrared electroluminescence emission from an n-InN nano dots/p-Si heterojunction structure [123].The brief and comparative discussion of the transport properties of simple InN/Si heterojunction is given.

Studies of the current–voltage characteristics of the n-InN ND/ p-Si heterostructures revealed the presence of good rectifying characteristics. Figure 17(a) shows the temperature dependent *I–V* characteristics of the heterojunction in the temperature range of 173–473 K. An excellent rectifying behaviour was observed at lower temperatures with an on/off ratio of 206 at 10 V. The deterioration observed in the rectifying nature at high temperature is due to thermally generated carrier tunnelling. The *I–V* curves were fitted by using the single carrier thermionic emission expression as given by equation (2). The zero bias (ZB) barrier heights are evaluated at each temperature, ZB BH (φ_b) and ideality factor η variations with temperature are shown in figure 17(b). A dependence of φ_b and η on the temperature is clearly observed which is attributed to the inhomogeneity at the interface [60]. A variation of the φ_b as a function of η with a linear correlation was also observed. The present behaviour can be associated with a non-uniform Schottky interface [60]. The BH depends on the electric field across the interface and consequently on the applied voltage, it is necessary to consider the standard field conditions. Under the flat band (FB) conditions, the electric field is zero across the interface. The capacitance–voltage (*C–V*) measurements performed [60] on the heterojunctions at 100 kHz in the temperature range of 173–473 K. The $BH_{(C-V)}$ values obtained are plotted in figure 17(b), and it can be seen that the FB BH is larger than the ZB BH at low temperature. The FB BH mirrors *C–V* BH with slight reduction in BH values at low temperature. This behaviour is attributed to the tunnelling and leakage through the dislocations and other defects resulting in high values of ideality factor ($\eta > 1$), which increases with decreasing temperature.

We have also carried out the comparative studies of transport properties of InN/p-Si heterojunctions. We have considered InN NRs and NDs grown on p-Si(1 0 0) substrates and compared with InN thin film grown on p-Si(1 1 1) substrates. The ideality factor and barrier height values obtained for various heterojunctions are listed in the table 2. It is observed that, a considerable increase in the ideality factors and reduction in barrier heights in the case of InN NRs/p-Si(1 0 0) and InN thin film/p-Si(1 1 1) heterojunctions when compared to the InN NDs/p-Si(1 0 0). Since the growth of InN NR and thin film are carried out at lower temperature (400 °C) compared the growth temperature (500 °C) of InN NDs. The poor crystalline quality and the interfacial defects leads the trap assisted tunnelling mechanism, which increases the ideality factors and lowers the barrier heights in the case of NRs and thin film heterojunctions.

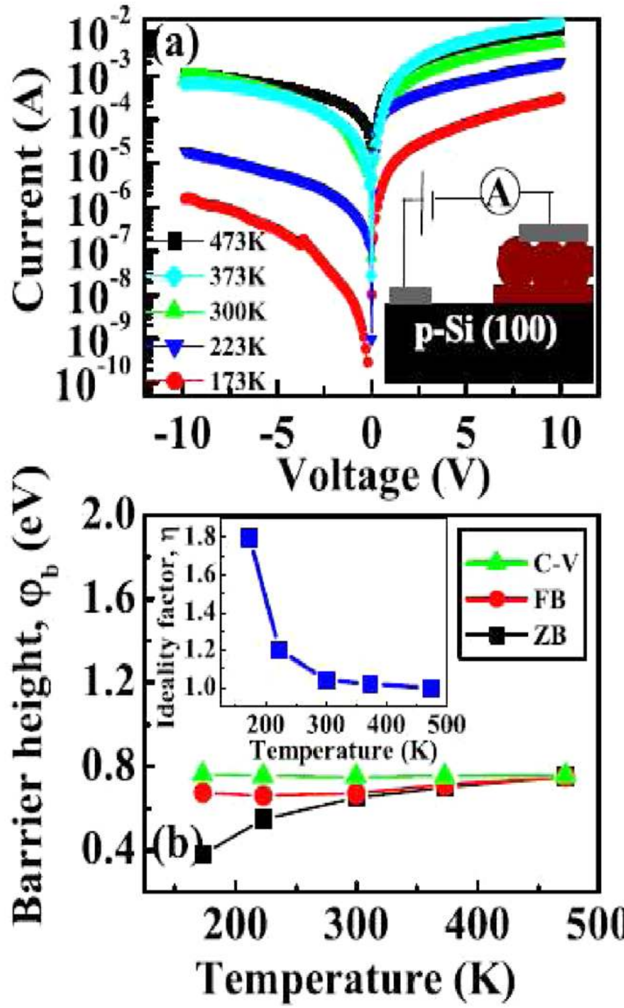

Figure 17. (a) Current versus voltage plots of the InN ND/p-Si diode at different temperatures. Inset shows schematic diagram of the device and measurement method. (b) Variation of ZB, FB, *C–V* barrier heights and ideality factor with temperature. Reproduced with permission from [60], copyright 2010 AIP Publishing LLC.

4.3. Current transport behaviour of InN/GaN heterostructures

The InN/GaN heterostructure system has several advantages for the development of electronic devices operating in THz frequency range [67]. These advantages includes the high rate of optical phonon emission in InN (2.5×10^{13} s^{-1}), high peak value of the steady state electron drift velocity in InN (5×10^7 cm s^{-1}) and large conduction band offset ensures the blocking of the conduction current over the barriers [67, 68]. Hence, studying the InN/GaN interface properties and calculating the conduction and valence band offsets between InN and GaN are very important in terms of fabrication of InGaN based devices.

Similar to metal–semiconductor interface, the semiconductor heterostructures exhibits the Schottky barrier at the interface due to the formation of conduction band offset. The concepts of band offset are directly transferable to the Schottky barrier height (SBH) problems and hence it is worthwhile to study the transport properties of the semiconductor heterostructure based Schottky junctions. Chen *et al* [124] studied the temperature dependent electrical transport properties of InN/GaN based Schottky junctions in the temperature range 300–400 K and reported nearly temperature independent barrier height (~1.25 eV) and ideality factor (~1.25). Wang *et al* [28] reported the Schottky barrier height of 0.94 eV at room temperature for the InN/GaN heterostructure using capacitance–voltage measurements. In this section we have fabricated InN/GaN Schottky junctions and studied the temperature dependent electrical transport properties. We have observed that the barrier height and the ideality factor are temperature dependent as estimated by thermionic field emission model. First we have grown InN/GaN heterostructures by PAMBE and then fabricated InN/GaN based Schottky junctions using standard devices processing steps like photolithography, dry etching, metallization and lift-off processes. Aluminium metal (thickness ~200 nm) was used as Ohmic contact to both GaN and InN layers. The *I–V* measurements were performed by taking contacts from two Al metals deposited on InN and GaN layers. Figure 18(a) shows the room temperature *J–V* (current density–voltage) measurement for the junction. The junction between InN and GaN exhibits a rectifying behaviour which suggests an existence of Schottky type behaviour at the junction [125].

Table 2. Ideality factor and barrier height values obtained for various InN/p-Si heterojunctions.

Samples with	Ideality factor, η	Barrier height, Φ (eV)
InN Nanodots/p-Si(1 0 0)	1.02	0.7
InN Film/p-Si(1 1 1)	2	0.4
InN Nanorods/p-Si(1 0 0)	2.2	0.38

To investigate in details, we have carried out temperature dependent *J–V (J–V–T)* measurements ranging from 200 to 500 K by steps of 50 K. Figure 18(b) shows the forward *J–V* characteristics as a function of temperature for the InN/GaN Schottky diode [125]. It is very clear from the *J–V–T* curve that at fixed bias the forward current increases with increasing temperature. In the present case, the GaN film is doped with silicon ($N_D \sim 1.4 \times 10^{18}$ cm^{-3}). The highly silicon doping on GaN resulted a narrow barrier width at the InN/GaN interface which helps in tunnelling of the carriers at the interface. This suggests that the current transport is primarily dominated by TFE mechanism, in which the carriers will tunnel through the barrier from GaN to InN at the interface. The values of the barrier height and the ideality factor (η) were calculated by fitting a line in the linear region of the forward *J–V* curves using the TFE model (equation (4)), as shown in figure 18(b). The value of φ_b, η and other electrical parameters such as E_{00} and E_0 while obtained from the fitting are given in table 3. It has been noticed that both the barrier height and the ideality factor are temperature dependent. Thus the results of our present investigation on temperature dependence of barrier height truly indicate the presence of inhomogeneous barrier height at the interface. The inhomogeneous SBH may be due to various types of defects that could be present at the interface [28, 126, 127]. Since in the present case, $E_{00}/kT \approx 1$, which suggests that TFE can be considered to be a more realistic model for the analysis of the electronic transport in InN/GaN heterostructure.

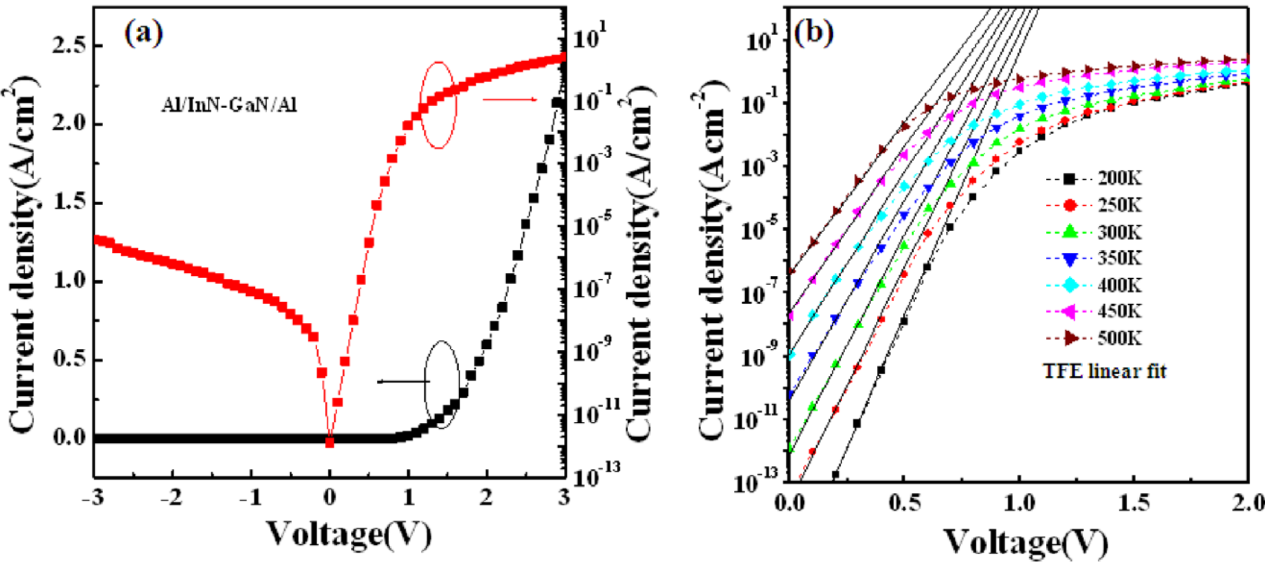

Figure 18. (a) The room-temperature J–*V* characteristics of InN/GaN Schottky junction. (b) The forward *J*–*V* characteristics with TFE fitting as a function of measurement temperature. Reproduced with permission from [125], copyright 2011 AIP Publishing LLC.

Table 3. The electrical parameters of InN/GaN Schottky diode [125].

Temp. (K)	E_{00} (meV)	E_{00}/kT	E_0 (meV)	φ_b (eV)	$\eta = E_0/kT$
200	24.12	1.39	26.00	1.40	1.50
250	25.85	1.19	29.20	1.42	1.35
300	28.17	1.08	31.50	1.43	1.21
350	30.16	0.99	34.50	1.44	1.14
400	34.00	0.98	38.00	1.47	1.10
450	37.00	0.95	41.50	1.49	1.07
500	40.00	0.92	45.00	1.50	1.04

4.4. Current transport behaviour of nonpolar InN/GaN heterostructures

The existence of Schottky barrier at InN/GaN interface could be explained in terms of large difference between the energy band gaps of InN and GaN. There are few reports on the transport studies on *c*-plane InN/GaN Schottky interfaces [124, 128]. However, the transport behaviour of nonpolar *a*-plane InN/GaN heterostructure interfaces is limited. In this section, we will discuss our results on the transport properties of nonpolar *a*-plane InN/GaN heterostructure. The inset of figure 19(a) shows the two aluminium (Al) metal contacts (Ohmic) fabricated on the InN and GaN. Figure 19(a) shows the room temperature *I–V* characteristic curve of nonpolar *a*-plane InN/GaN heterostructure Schottky diode [88]. The rectifying behaviour of the *I–V* curve indicates the existence of Schottky barrier at the InN and GaN interface. The linear region of the forward *I–V* curves was fitted using the TE model, in order to calculate the values of Schottky barrier height (φ_b) and the ideality factor (η) for nonpolar InN/GaN junction. It was found that η and φ_b values ranging from 1.65 and 0.83 eV (500 K) to 4.1 and 0.4 eV (150 K), respectively as shown in the figure 19(b). The values of φ_b increases and η decreases with increasing temperature, indicating the inhomogeneous nature of nonpolar InN/GaN interface.

The inhomogeneous SBH could arise due to the various types of defects present at the InN/GaN interface [126, 127]. The earlier report with temperature dependent barrier height and ideality factor in Pt/a-plane GaN Schottky diode was explained in terms of surface defects in nonpolar *a*-plane GaN [129]. The Richardson plot of saturation current has been used to in order to evaluate the barrier height (φ_b). There are two linear regions were observed in the temperature region 150–300 K and 350–500 K. The values of Richardson's constant (A^*) were found to be much lower than the theoretical value of 24 A cm^{-2} K^{-2} for n-GaN. The inhomogeneous nature of Schottky barrier at the InN/GaN interface was explained by considering the Gaussian distribution of barrier heights [130, 131], which can be written as,

$$P(\varphi_b) = \frac{1}{\sigma_s\sqrt{2\pi}} \exp\left[-\frac{(\varphi_b - \overline{\varphi_b})^2}{2\sigma_s^2}\right], \quad (8)$$

where $1/\sigma_s\sqrt{2\pi}$ is the normalization constant and $\overline{\varphi_b}$ and σ_s are the mean and standard deviation of barrier height respectively. Considering Gaussian distribution of barrier height the effective barrier height, φ_b given by the expression,

$$\varphi_b = \overline{\varphi_{b0}} - \frac{q\sigma_s^2}{2kT}. \quad (9)$$

Here, $\overline{\varphi_{b0}}$ is the zero bias mean barrier height. Considering the barrier height inhomogeneities, the conventional Richardson plot is modified as follows

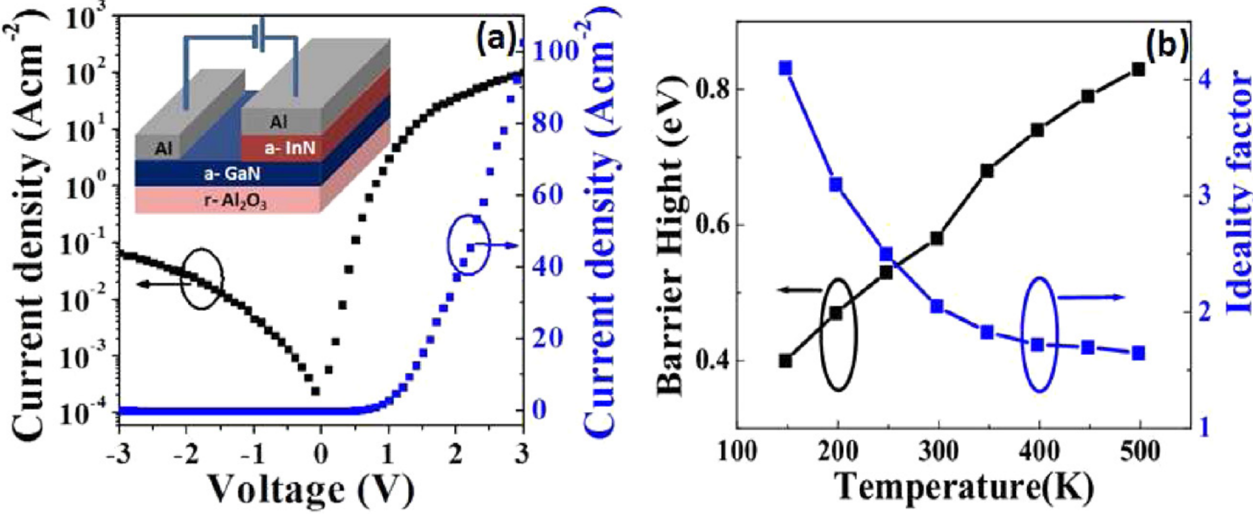

Figure 19. (a) The room temperature *I–V* characteristics of the nonpolar *a*-plane InN/GaN Schottky junction. (b) The temperature dependent variation of barrier height and the ideality factor. Reproduced with permission from [88], copyright 2012 AIP Publishing LLC.

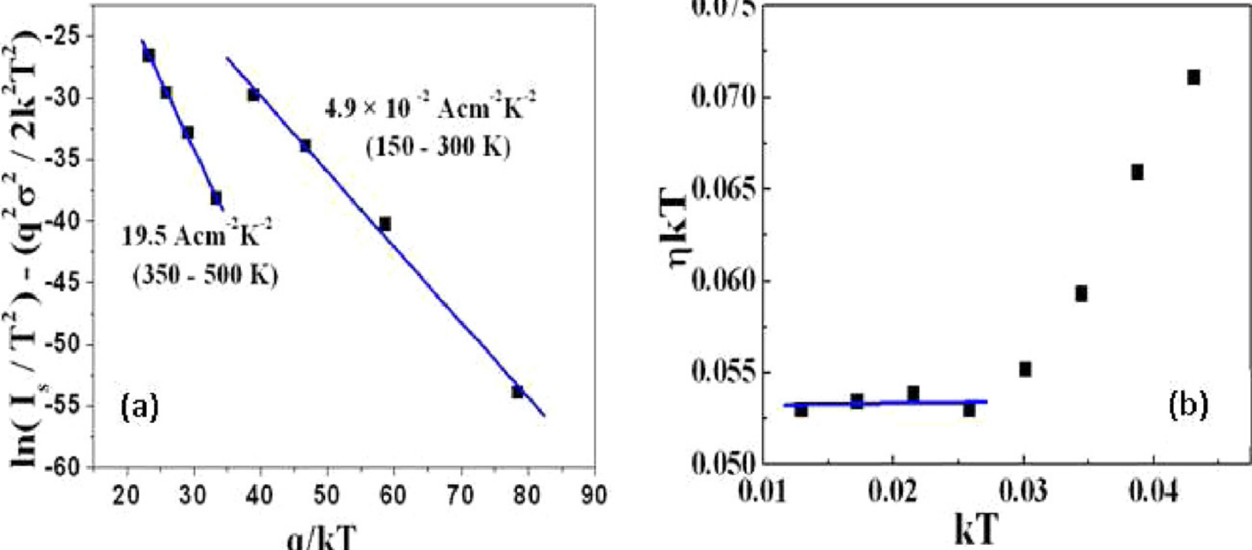

Figure 20. (a) Modified Richardson plot of $\ln(I_s/T^2) - q^2\sigma^2/2k^2T^2$ versus q/kT. (b) Plot of ηkBT as a function of kBT. Reproduced with permission from [88], copyright 2012 AIP Publishing LLC.

$$\ln\left(\frac{I_s}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\overline{\varphi_{b0}}}{kT}. \quad (10)$$

Figure 20(a) shows the modified Richardson plot considering the Gaussian distribution. In the first region (300–500 K), the values of BH ($\overline{\varphi_b}$) and effective Richardson constant (A^*) were found to be 1.15 eV and 19.5 A cm^{-2} K^{-2}, respectively. The calculated Richardson constant value in the temperature range of 350–500 K is very close to the theoretical value of 24 A cm^{-2} K^{-2} for n-type GaN. This indicates that at higher temperatures (350–500 K) the current transport is dominated by TE mechanism. The values of BH ($\overline{\varphi_b}$) and effective Richardson constant (A^*) were found to be 1.6 eV and 25.8 A cm^{-2} K^{-2}, respectively for polar *c*-plane InN/GaN [128]. The reduction in barrier height in nonpolar *a*-plane InN/GaN with respect to the polar *c*-plane InN/GaN was explained in terms of the absence of polarization field at the interface. The value of A^* in the temperature range of 150–300 K shows the large deviation indicating that the TE mechanism does not dominate in this region. Figure 20(b) shows $E_0 = \eta kT$ versus kT plot for the nonpolar *a*-InN/GaN Schottky diode. The value of E_0 is independent of temperature at the low temperature indicating that the FE dominates in the range of 150–500 K [132]. The carriers do not have enough energy to surmount the barrier at the low temperature and they tunnel through the defects at the interface.

4.5. Transport studies of Au/GaN heterostructures

The performance of the GaN based optoelectronic devices are limited by the nature of the metal contacts and hence the understanding of the electrical transport behaviour of metal contacts

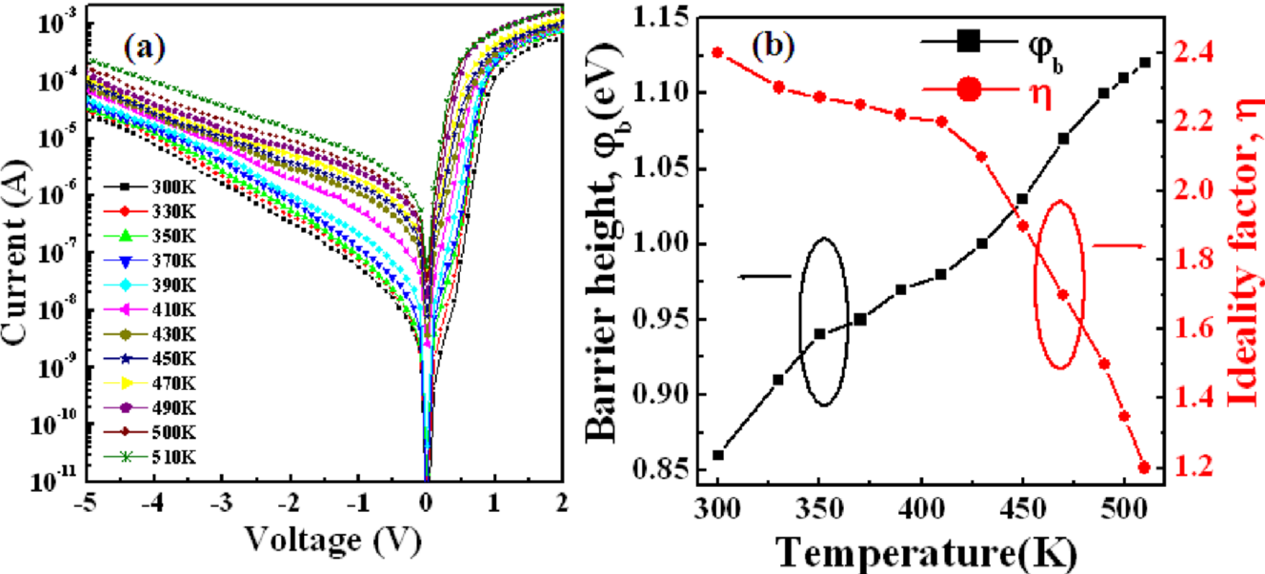

Figure 21. (a) The *I–V* characteristics of Au/GaN Schottky diodes at different temperatures. (b) The temperature dependence of the barrier height and the ideality factor. Reproduced with permission from [136], copyright 2012 John Wiley and Sons.

to GaN is an important subject. Several groups have reported the electrical transport behaviour of n-GaN Schottky diodes by taking different metal contacts. Ping *et al* [133] fabricated Pd/GaN Schottky diodes and reported the barrier height of 0.94 and 1.07 eV using *I–V* and *C–V* measurements, respectively. Hacke *et al* [134] reported the Schottky barrier heights of 0.84 eV and 0.94 eV using *I–V* and *C–V* measurements, respectively, for Au/GaN Schottky diodes. In another study on Au/n-GaN Schottky diode, Khan *et al* [135] reported the values of barrier height as 0.91 and 1.01 eV using *I–V* and *C–V* measurements, respectively. In this section we have reported the temperature dependent electrical transport properties of Au/GaN Schottky diodes. High quality GaN film on sapphire substrate were grown and studied the temperature dependent electrical transport properties of Au/GaN Schottky diodes in the temperature range of 300–510 K. The barrier height and the ideality factor were calculated from *I–V* characteristic based on thermionic emission which found to be temperature dependent. The temperature dependent of barrier height was interpreted by assuming the existence of a Gaussian distribution of barrier heights at the Au/GaN interface.

Figure 21(a) shows the temperature dependent *I–V* characteristics of the Au/GaN Schottky diode [136]. The diameter of the Au Schottky contact was 600 μm. The rectifying behaviour of the *I–V* curve indicates the existence of Schottky barrier at the InN and GaN interface. It is clear from the figure that the forward current of the diode at a fixed bias increases with increasing the measurement temperature. This indicates that the current is induced by the thermionic emission. The values of the SBH (φ_b) and the ideality factor (η) for the junction were calculated as functions of the measurement temperature by fitting a line in the linear region of the forward *I–V* curves using the thermionic emission model as described in earlier section. The dependence of the barrier height and the ideality factor is depicted in figure 21(b) [136]. It is found that the barrier height increased from 0.86 to 1.12 eV while the ideality factor decreased from 2.4 to 1.2 with the increase in measurement temperature from 300 to 510 K. Such temperature dependence of φ_b and η is may be due to the existence of surface inhomogeneities in the GaN semiconductor layer [137].

For the evaluation of the barrier height, Richardson plot of the saturation current was utilized. Equation (3) can be rewritten as

$$\ln\left(\frac{I_s}{T^2}\right) = \ln(AA^*) - \frac{q\varphi_b}{kT}. \tag{11}$$

The conventional Richardson's plot of $\ln(I_s/T^2)$ versus $1/kT$ was obtained and is shown in figure 22(a) [136]. From the linear fit to the plot, the Richardson's constant and barrier height were calculated to be 3.23×10^{-5} A cm^{-2} K^{-2} and 0.51 eV respectively. The value of Richardson constants obtained from the conventional Richardson plot is much lower than the theoretical value, which is 24 A cm^{-2} K^{-2}, suggested the formation of an inhomogeneous barrier height and potential fluctuations at the interface. In order to understand the lateral inhomogeneities of the barrier height at the interface, Sullivan *et al* [138] and Tung [139, 140] have treated the system consists of laterally inhomogeneous patches of different barrier heights, in which the patches of lower barrier height yields a larger ideality factor and vice versa. Mamor *et al* [141] suggested the lateral inhomogeneity of the barrier height can be attributed to the presence of defects at the interface.

Figure 22(b) shows $\ln(I_s/T^2) - q^2\sigma_s^2/2k^2T^2$ versus q/kT plot, so called modified Richardson plot [136], which is derived by considering Gaussian distribution of barrier heights to describe the inhomogeneous nature at the interface. It can be seen that the modified Richardson plot has quite good linearity over the whole temperature range. From the modified plot, the Richardson's constant and barrier height were calculated to be 38.8 A cm^{-2} K^{-2} and 1.47 eV respectively. The value of Richardson constant obtained from the modified Richardson

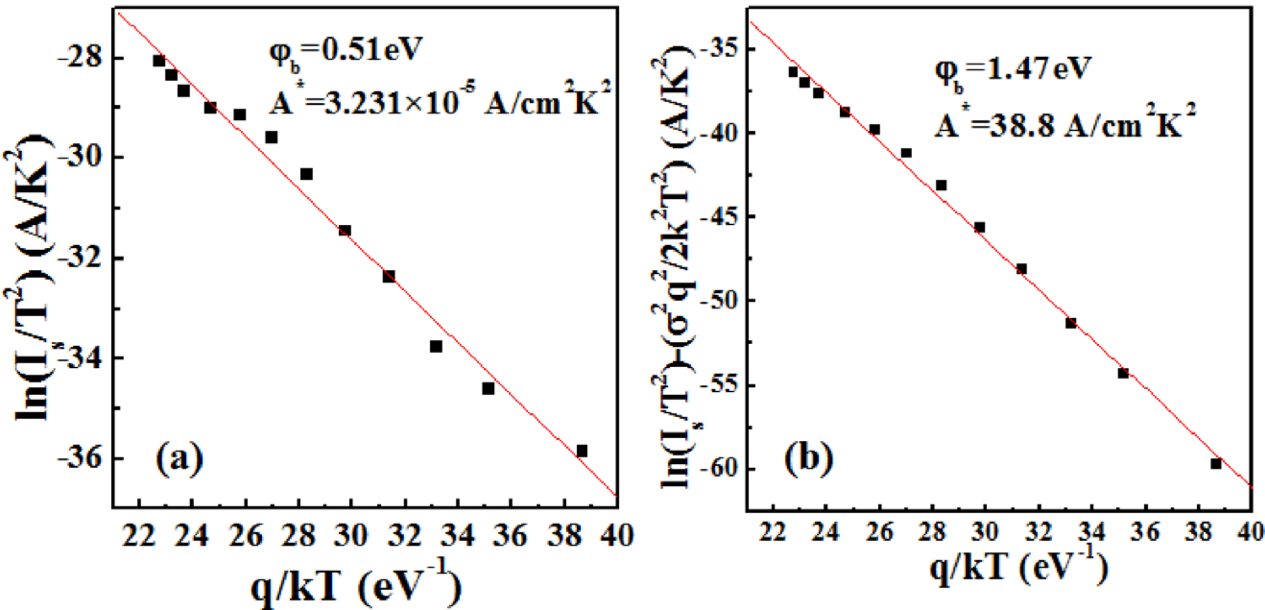

Figure 22. (a) The Richardson plot of $\ln(I_s/T_2)$ versus $1/kT$ for Au/GaN Schottky diodes. (b) The modified Richardson plot of $\ln(I_s/T^2) - q^2\sigma^2/2k^2T^2$ versus q/kT. Reproduced with permission from [136], copyright 2012 John Wiley and Sons.

plot is nearly close to the theoretical value of 26.4 A cm^{-2} K^{-2}. Hence, the temperature dependence of *I–V* characteristics of the Au/GaN Schottky diode shows the existence of a Gaussian distribution of barrier height at the Au and GaN interface.

5. Conclusions

In summary, we presented the studies on the growth and properties of group III-nitride heterojunctions. Here, the discussion has been carried out on the growth and properties of GaN/Si, InN/Si, Polar InN/GaN, and nonpolar InN/GaN heterostructures. Followed by studies on band offsets of III-nitride semiconductor heterostructures which is carried out by using XPS studies. Current transport mechanisms of heterostructures are also discussed.

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