Received 29 December 2014; revised 8 March 2015; accepted 10 April 2015. Date of publication 20 April 2015; date of current version 19 June 2015.
The review of this paper was arranged by Editor C. Surya.

*Digital Object Identifier 10.1109/JEDS.2015.2424686*

# Analytical Modeling of Flicker Noise in Halo Implanted MOSFETs

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This work was supported in part by the DST Fast Track Scheme for Young Scientists, in part by Ramanujan Fellowship, in part by the Indian Institute of Technology Kanpur Initiation Grant, and in part by Semiconductor Research Corporation under Research 2462.

**ABSTRACT** An improved analytical model for flicker noise (1/*f* noise) in MOSFETs is presented. Current models do not capture the effect of high-trap density in the halo regions of the devices, which leads to significantly different bias dependence of flicker noise across device geometry. The proposed model is the first compact model implementation capturing such effect and show distinct improvements over other existing noise models. The model is compatible with BSIM6, the latest industry standard model for bulk MOSFET, and is validated with measurements from 45-nm low-power CMOS technology node.

**INDEX TERMS** BSIM6, halo doping, flicker noise, compact model.

## I. INTRODUCTION

For low power technologies driven by challenging targets for off-state leakage current without compromising performance, strong halo implants are necessary for suppressing parasitic 2-D electrostatics for the minimum length device. However, such strong halo implants have been found to be detrimental to analog performance [1], [2] including 1/f noise [3], [4] in particular for long channel devices [5]. The degradation of 1/f noise has been attributed to extra trap states generated due to implantation process [3], and/or threshold voltage variation along the channel [4]. Due to this reason noise behavior in strong pocket devices are significantly different than in uniformly doped devices. Existing compact models that can successfully capture noise behavior in uniformly doped devices are no longer valid.

Fig. 1 shows the measured median (of 21 different sites in wafer) drain current flicker noise power spectral density (PSD) normalized to channel width for long and short channel devices for 45nm low power CMOS technology node [6]. Note that contrary to uniform channel doped noise, the strong pocket devices show no impact of channel length scaling for 1/f noise in the subthreshold or near-threshold-voltage region. This is a key factor that needs to be understood as analog designs are targeting low power regions of operation. As the drain current is increased by increasing the gate-voltage, the long channel device further show anomalous bias dependence through a sudden decrease in slope. The short channel device does not show this characteristic. Such behavior cannot be captured by existing noise models based on uniformly doped channel devices [7] (see Fig. 1). Although a noise model specific to halo devices was earlier proposed by Wu *et al.* [4] based on a non-uniform threshold voltage distribution using the unified noise model, it adds the noise contributions from the different regions with equal proportions. Such formulation might lead, in certain cases, to excess contribution of noise from pocket part in strong inversion, or excess contribution from channel part for lower bias. Also that model does not consider the impact of higher trap densities (in halo regions) on noise typical to pocket implant process, and is valid only in strong inversion. In this work, we will discuss the physical mechanisms behind the bias dependence for halo implanted devices and present an analytical model, valid from weak inversion (WI) to strong inversion (SI), that can capture the behavior across

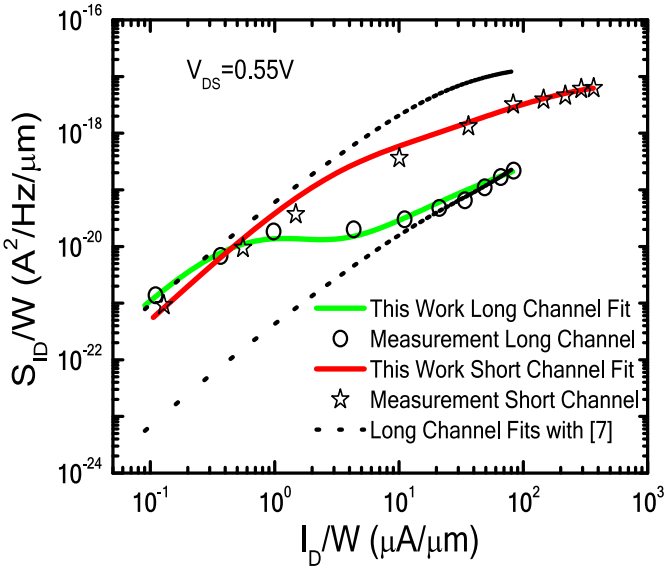


**FIGURE 1.** Drain current flicker noise power spectral density versus drain current at $V_{DS} = 0.55$ V, both normalized to channel width. Measurements are from the same technology as in [6] and show complex dependency on gate voltage, especially for long channel device. Weak inversion noise is dominated by contributions from halo regions and therefore there is no impact of length scaling on $1/f$ noise.

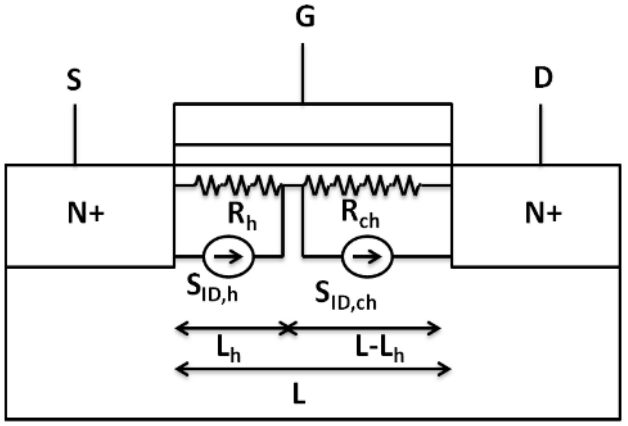


**FIGURE 2.** Representation of MOSFET for noise modeling. Channel length $L$ can be divided into two parts—the halo region of length $L_h$ with doping $N_h$ and the channel region of length $L$-$L_h$ with doping $N_{ch}$.

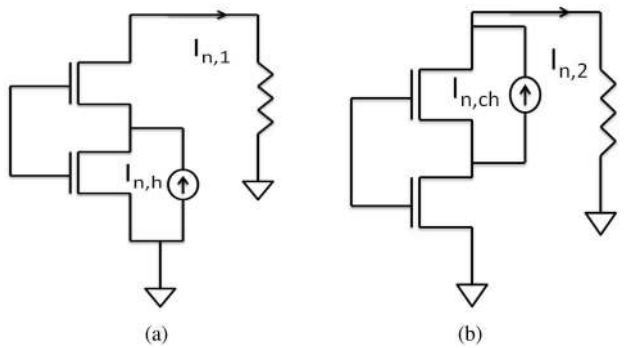


**FIGURE 3.** Small signal analysis of two transistor noise circuit. Principle of superposition is used to obtain total noise from individual noise contributions. (a) Noisy halo transistor and noiseless channel transistor. (b) Noisy channel transistor and noiseless halo transistor.

length considering the impact of both non-uniform threshold voltage and increased trap density. The model is compatible with BSIM6 MOS model, which is the latest industry standard compact model of bulk MOSFET [8]–[10].

## II. ANALYTICAL FLICKER NOISE MODEL

### A. MODEL FORMULATION

Starting with the earlier Langevin method for flicker noise modeling, there exist other approaches like equivalent circuit method, impedance field method, Klaassen Prins (KP) approach, etc. [11]–[13]. The presented formulation is based on small signal approach, which is similar to the impedance field method. The halo doped transistor can be represented as in Fig. 2, where the total length L is segmented into two parts: a region of higher doping of length $L_h$ with equivalent resistance $R_h$, noise PSD $S_{ID,h}$ and another low doped region of length L-$L_h$ with resistance $R_{ch}$ and noise PSD $S_{ID,ch}$. In a very crude form (neglecting transistor transconductance), overall drain current noise PSD ($S_{ID}$) can be expressed as [14],

$$S_{ID} = S_{ID,h}\left[\frac{R_h}{R_h + R_{ch}}\right]^2 + S_{ID,ch}\left[\frac{R_{ch}}{R_h + R_{ch}}\right]^2 \quad (1)$$

We have demonstrated earlier that (1) can be implemented by simple two transistor subcircuit model where resistances of channel and halo regions are calculated by SPICE [14]. However, such an implementation cannot be used for a practical industry standard compact model formulation since it degrades the simulation speed as well as complicates model parameter extraction procedure. Here we will present a complete analytical model that can successfully reproduce the series transistor noise behavior without above limitations. Firstly, the I-V parameters of the family of devices under test are extracted. For the noise modeling, it is now assumed that the transistor is composed of two transistors, channel transistor of length L-$L_h$ and halo transistor of length $L_h$ connected in series and carries same current ($I_{DS}$) as in single transistor configuration. The individual contribution of the halo and channel transistors to overall noise is obtained using small signal analysis and principle of superposition.

From Fig. 3(a), the drain current noise PSD due to halo transistor is obtained by assuming channel transistor to be noiseless. Using small signal analysis,

$$I_{n1} \simeq I_{n,h}\frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \quad (2)$$

$$S_{ID,1} = S_{ID,h}\left[\frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}}\right]^2 \quad (3)$$

where $g_{m,ch}$, $g_{d,ch}$ are the transconductance and output conductance of channel transistor and $g_{d,h}$ is the transconductance of the halo transistor. Similarly from Fig. 3(b),

the noise PSD due to the channel transistor is expressed as

$$I_{n2} \simeq I_{n,ch}\frac{g_{d,h}}{g_{m,ch}+g_{d,ch}+g_{d,h}} \tag{4}$$

$$S_{ID,2} = S_{ID,ch}\left[\frac{g_{d,h}}{g_{m,ch}+g_{d,ch}+g_{d,h}}\right]^2 \tag{5}$$

Total drain current noise PSD becomes,

$$S_{ID} = S_{ID,1} + S_{ID,2} \tag{6}$$

$$= S_{ID,h}\left[\frac{g_{m,ch}+g_{d,ch}}{g_{m,ch}+g_{d,ch}+g_{d,h}}\right]^2 + S_{ID,ch}\left[\frac{g_{d,h}}{g_{m,ch}+g_{d,ch}+g_{d,h}}\right]^2 \tag{7}$$

$$= S_{ID,h}.CF_h + S_{ID,ch}.CF_{ch} \tag{8}$$

We refer to the multiplying factors to $S_{ID,h}$ and $S_{ID,ch}$ in (7) as contribution factors (CF). From [15],

$$g_{d,ch} = 2n_q\mu C_{ox}\frac{W}{L-L_h}V_t q_{d,ch} \tag{9}$$

$$g_{d,h} = 2n_q\mu C_{ox}\frac{W}{L_h}V_t q_{d,h} \tag{10}$$

$$g_{m,ch} = 2\mu C_{ox}\frac{W}{L-L_h}V_t(q_{s,ch}-q_{d,ch}) \tag{11}$$

where $n_q$, $\mu$, $C_{ox}$, and $V_t$ are the slope factor, effective mobility, oxide capacitance per unit area and thermal voltage respectively. $q_{s,ch}$, $q_{d,ch}$, $q_{s,h}$ and $q_{d,h}$ are the normalized inversion charge densities at the source and drain ends of channel and halo transistor respectively. $q_{sh}$ and $q_{d,ch}$ are obtained from analytical solution of BSIM6 [16] charge equation given by (12), where pinch-off potential ($\psi_p$, normalized to thermal voltage $V_t$) is given by (13) and is calculated independently for the two transistors using source potential $v_{ch} = v_s$ and $v_{ch} = v_d$ (effective drain potential) respectively. $v_g$, $v_{fb}$, $\phi_f$ and $\gamma$ in these equations are the normalized gate voltage, flat band voltage, bulk potential and body factor, respectively and $\psi_{p0}$ is the approximation of pinch-off potential when it is close to zero. To calculate $q_{d,h}$ and $q_{s,ch}$, the fact that the same current flows in one transistor and two transistor noise equivalent configuration is used,

$$i_h = \frac{I_{DS}}{-2n_q\mu C_{ox}\frac{W}{L_h}V_t^2} = \left(q_{s,h}^2+q_{s,h}\right)-\left(q_{d,h}^2+q_{d,h}\right) \tag{14}$$

$$i_{ch} = \frac{I_{DS}}{-2n_q\mu C_{ox}\frac{W}{L-L_h}V_t^2} = \left(q_{s,ch}^2+q_{s,ch}\right)-\left(q_{d,ch}^2+q_{d,ch}\right) \tag{15}$$

where $i_h$ and $i_{ch}$ are the normalized drain current of halo and channel transistor respectively. Since $I_{DS}$ is known from DC modeling, the above equations are solved for,

$$q_{d,h} = -\frac{1}{2}+\frac{1}{2}\sqrt{1+4\left(q_{s,h}^2+q_{s,h}-i_h\right)} \tag{16}$$

$$q_{s,ch} = -\frac{1}{2}+\frac{1}{2}\sqrt{1+4\left(q_{d,ch}^2+q_{d,ch}+i_{ch}\right)} \tag{17}$$

### B. NOISE SOURCE

The source of flicker noise in MOSFETs is attributed to mobility fluctuation and/or carrier number fluctuation [17]–[19]. There exist popular models which unifies the two approaches [7], [20], [21]. Here we have used the unified model presented in [20] (which has been widely used in industry standard bulk MOSFET models [22]–[24]) for halo and channel transistors separately, where $S_{ID}$ is expressed as

$$S_{ID,h} = \frac{kTI_{DS}^2}{\gamma fWL_h^2}\int_0^{L_h}\frac{N_{t,h}^*(E_{F_n})}{N_h^2}dx \tag{18}$$

$$S_{ID,ch} = \frac{kTI_{DS}^2}{\gamma fW(L-L_h)^2}\int_{L_h}^{L}\frac{N_{t,ch}^*(E_{F_n})}{N_{ch}^2}dx \tag{19}$$

where apparent trap density $N_{t,ch(h)}^*(E_{F_n}) = A_{ch(h)} + B_{ch(h)}N_{ch(h)} + C_{ch(h)}N_{ch(h)}^2$, $A$, $B$, $C$ are the noise parameters, $\gamma$ is the tunneling parameter, $k$ is the Boltzmann constant and $T$ is the temperature. It is important to note that $S_{ID,h}$ and $S_{ID,ch}$ are in explicit form since (18) and (19) can be expressed as a function of $q_{s,h}$, $q_{d,h}$ and $q_{s,ch}$ and $q_{d,ch}$ respectively [25]. Also note that $S_{ID}$ in the halo region might be locally higher than in the channel region due to increased trap density which is captured by the noise parameters of the halo transistor. Hence formulation of $S_{ID}$ is based on the local trap density, inversion charge densities specific to the region that generates the noise as well as the length of the region. Using (18) and substituting (16), (17), $q_{s,h}$, $q_{d,ch}$ in (7) gives the overall PSD.

## III. RESULTS AND DISCUSSION

The model is validated with the measurements at 45nm CMOS technology. Validation is carried for both long and short channel device at $V_{DS} = 0.55$V. Fig. 1 shows the model data overlay for long and short channel transistors. Unlike for the short channel case, long channel device shows significant bias dependency, and the model is able to accurately reproduce the experimental characteristics both for the long and short channel devices. For the better understanding,

$$\ln(q_i) + \ln\left[\frac{2n_q}{\gamma}\left(q_i\frac{2n_q}{\gamma}+2\sqrt{\psi_p-2q_i}\right)\right] + 2q_i = \psi_p - 2\phi_f - v_{ch} \tag{12}$$

$$\psi_p = \begin{cases} -\ln\left[1-\psi_{p0}+\left(\frac{v_g-v_{fb}-\psi_{p0}}{\gamma}\right)^2\right] & \text{if } v_g - v_{fb} < 0 \\ 1-e^{-\psi_{p0}}+\left[\sqrt{v_g-v_{fb}-1+e^{-\psi_{p0}}+\left(\frac{\gamma}{2}\right)^2}-\frac{\gamma}{2}\right]^2 & \text{otherwise} \end{cases} \tag{13}$$

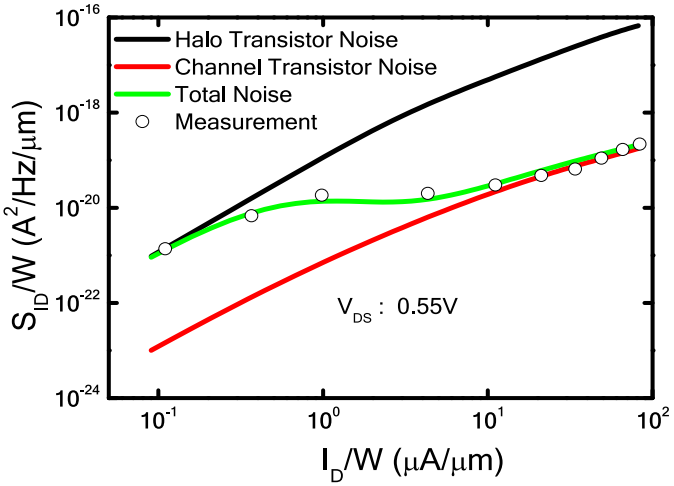


**FIGURE 4.** **Model validation with long channel device: $S_{ID}$ versus $I_{DS}$ at $V_{DS} = 0.55$ V. $S_{ID}$ asymptotically follows halo transistor noise in weak inversion and channel transistor noise in strong inversion.**

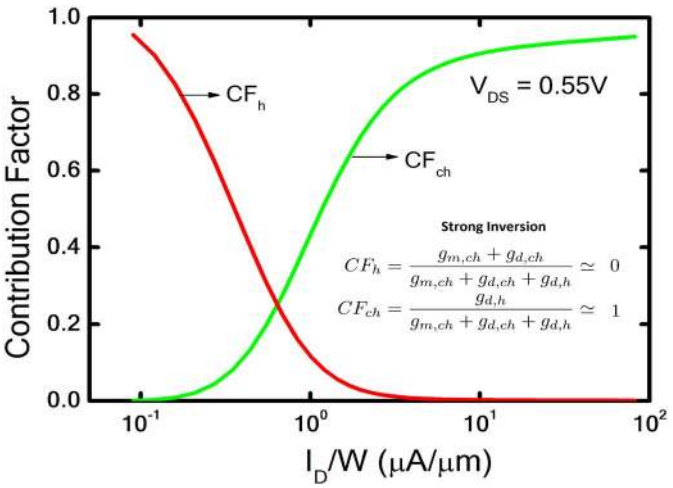


**FIGURE 5.** **Contribution factor of halo and channel transistors versus drain current. In weak inversion, $CF_h >> CF_{ch}$, and thus $S_{ID}$ is dominated by the noise from the halo region [see (8)]. On the other hand, $CF_h$ falls rapidly in the strong inversion leading to the negligible contribution from halo region in $S_{ID}$. The role of CF in this model is similar to that of impedance field [11], which is responsible for noise propagation from a point in the channel to the drain terminal. Note that [4] adds halo and channel contribution with equal weights, therefore will overestimate noise in strong inversion.**

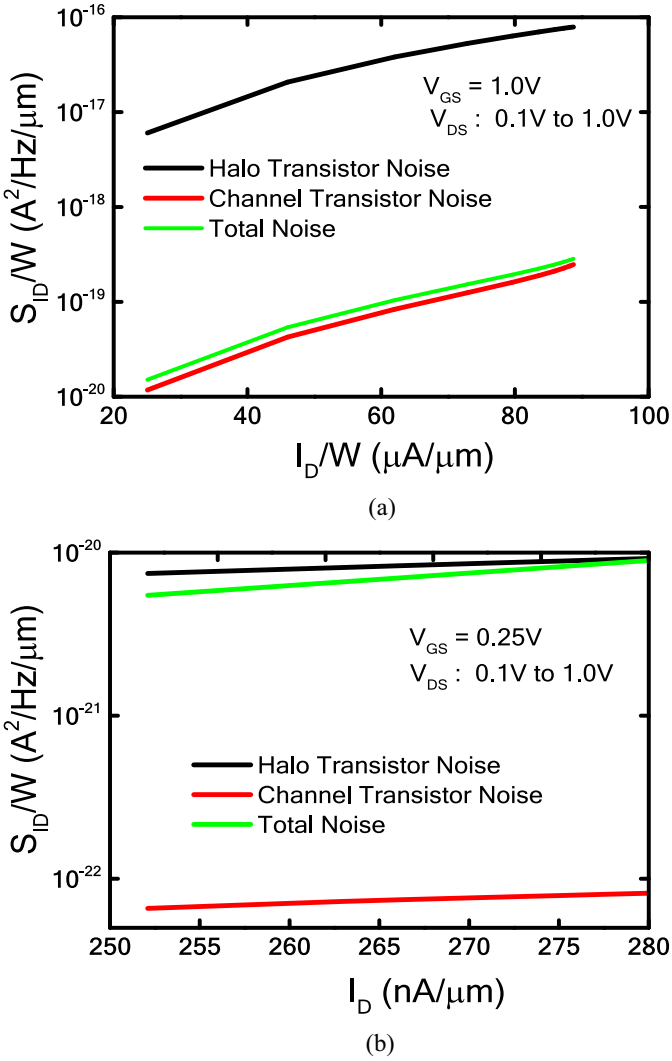


**FIGURE 6.** **Simulated drain current noise spectral density versus drain current for constant gate voltage and varying $V_{DS}$ from 0.1 to 1.0 V for the long channel device. (a) $V_{GS} = 1.0$ V. (b) $V_{GS} = 0.25$ V. (a) High gate voltage strongly inverts both halo and channel regions. However, resistance of the channel region is larger as its length is large compared to the halo region, as a result total noise is dominated by the channel region noise. (b) Halo region offers much higher resistance than the channel part due to its high threshold voltage and hence the total noise is determined by the noise of the halo transistor.**

long channel noise PSD along with the halo and channel transistor PSD is shown in Fig. 4. Although the devices have halo doping at source and drain ends, we found that two transistor sub-circuit implementation is sufficient to capture the bias and channel length dependencies for noise modeling and simpler for parameter extraction than a three transistor implementation. Due to higher doping in halo MOSFET, it has higher threshold voltage than the channel counterpart which leads to significantly lower inversion charge density especially at low gate voltages. For a given current, $S_{ID}$ is inversely proportional to the square of inversion charge density, and therefore halo transistor will have much higher $S_{ID}$ compared to the channel transistor. Furthermore, in WI $g_{d,h} << g_{m,ch}$ (as $q_{s,ch} >> g_{d,h}$ since halo transistor has higher threshold voltage) leading to

$$CF_h = \frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \simeq 1 \tag{20}$$

$$CF_{ch} = \frac{g_{d,h}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \simeq 0 \tag{21}$$

Since the contributed noise is the product of CF and $S_{ID}$, overall noise is dominated by halo transistor noise in WI. From (8) it follows that,

$$S_{ID} \simeq S_{ID,h} \tag{22}$$

While the CF for the halo transistor falls rapidly, the CF for the channel transistor rises sharply as the region of operation moves from WI to SI as shown in Fig. 5, and as a result,

the channel transistor noise becomes the dominant component of the noise in SI. The model presented in [4] adds the individual contributions with equal weights, and therefore cannot model the complex noise characteristics. Fig. 1 also shows the $S_{ID}$ vs drain current for short channel device. It is interesting to observe that short channel device does not shows the bias dependency like the long channel device. This can be explained by the fact that the length of halo transistor is comparable with the length of channel transistor for short channel device, making the transition smoother from halo dominated region to channel dominated region. For the sake of completeness, the model behavior with different drain voltage is also studied. Fig. 6 shows the drain current noise PSD vs drain current for two gate voltages, $V_{GS} = 1V$ in Fig. 6(a) and $V_{GS} = 0.25V$ in Fig. 6(b), and varying drain voltage. For the entire drain bias range (0.1V to 1.0V), total noise is mainly due to the channel transistor noise in Fig. 6(a). This could be understood as follows: high gate voltage strongly inverts both channel and halo regions, however channel region offers higher resistance due to its larger length (as compared to halo region length) leading to $CF_{ch} >> CF_h$ and hence $S_{ID,ch} >> S_{ID,h}$ from (8). Similarly for the low gate voltages, total noise is dominated by the noise of the halo region as seen in Fig. 6(b), since resistance of the halo region is much higher than the resistance of the channel region due to its high threshold voltage.

## IV. CONCLUSION

An analytical model of flicker noise for halo implanted MOSFET is presented. The impact of halo regions associated with the device on flicker noise is modeled using a separate MOSFET connected in series with the channel transistor. The model is a significant improvement over existing models in capturing bias and channel length dependencies of noise in devices employing strong halo technology. The model is amenable to be integrated with BSIM6 and provides an excellent solution to model the 1/f noise for the low power CMOS technology with high quality analog capability.

## REFERENCES

[1] K. M. Cao *et al.*, "Modeling of pocket implanted MOSFETs for anomalous analog behavior," in *IEDM Tech. Dig.*, Washington, DC, USA, 1999, pp. 171–174.
[2] A. S. Roy, S. P. Mudanai, and M. Stettler, "Mechanism of long-channel drain-induced barrier lowering in halo MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 979–984, Apr. 2011.
[3] A. K. M. Ahsan and S. Ahmed, "Degradation of 1/f noise in short channel MOSFETs due to halo angle induced VT non-uniformity and extra trap states at interface," *Solid-State Electron.*, vol. 50, nos. 11–12, pp. 1705–1709, 2006.
[4] J.-W. Wu *et al.*, "Pocket implantation effect on drain current flicker noise in analog nMOSFET devices," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1262–1266, Aug. 2004.
[5] P. Srinivasan and S. Dey, "New and critical aspects of 1/f noise variability in advanced CMOS SoC technologies," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 19.3.1–19.3.4.
[6] K. Benaissa *et al.*, "New cost-effective integration schemes enabling analog and high-voltage design in advanced CMOS SoC technologies," in *Proc. Symp. VLSI Technol. (VLSIT)*, Honolulu, HI, USA, 2010, pp. 221–222.
[7] K. Hung, P. K. Ko, C. Hu, and Y. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990.
[8] Y. S. Chauhan *et al.*, "BSIM6: Analog and RF compact model for bulk MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 234–244, Feb. 2014.
[9] H. Agarwal *et al.*, "Analytical modeling and experimental validation of threshold voltage in BSIM6 MOSFET model," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 240–243, May 2015.
[10] S. Khandelwal *et al.*, "Modeling STI edge parasitic current for accurate circuit simulations," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, to be published.
[11] A. S. Roy, C. C. Enz, and J. M. Sallese, "Noise modeling methodologies in the presence of mobility degradation and their equivalence," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 348–355, Feb. 2006.
[12] A. Cappy and W. Heinrich, "High-frequency FET noise performance: A new approach," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 403–409, Feb. 1989.
[13] F. M. Klaassen, "Characterization of low 1/f noise in MOS transistors," *IEEE Trans. Electron Devices*, vol. 18, no. 10, pp. 887–891, Oct. 1971.
[14] N. Paydavosi *et al.*, "Flicker noise in advanced CMOS technology: Effects of halo implant," in *Proc. IEEE Eur. Solid-State Device Res. Conf. (ESSDERC)*, Bucharest, Romania, 2013, pp. 238–241.
[15] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Chichester, U.K.: Wiley, 2006.
[16] H. Agarwal *et al.*, "Recent enhancements in BSIM6 bulk MOSFET model," in *Proc. IEEE Int. Conf. Simulat. Semicond. Process. Devices (SISPAD)*, Glasgow, U.K., 2013, pp. 53–56.
[17] A. L. McWhorter, "1/f noise and germanium surface properties," in *Semiconductor Surface Physics*. Philadelphia, PA, USA: Univ. Pennsylvania Press, 1957, pp. 207–228.
[18] F. N. Hooge, "1/f noise is no surface effect," *Phys. Lett. A*, vol. 29, no. 3, pp. 139–140, 1969.
[19] R. Jindal, "Compact noise models for MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2051–2061, Sep. 2006.
[20] K. Hung, P. K. Ko, C. Hu, and Y. Cheng, "A physics-based MOSFET noise model for circuit simulators," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 1323–1333, May 1990.
[21] R. Jayaraman and C. Sodini, "A 1/f noise technique to extract the oxide trap density near the conduction band edge of silicon," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1773–1782, Sep. 1989.
[22] (2013). *BSIM4 Technical Manual*. [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIM4
[23] G. Gildenblat, *Compact Modeling: Principles, Techniques and Applications*. Dordrecht, The Netherlands: Springer, 2010.
[24] H. Agarwal, S. Khandelwal, Y. S. Chauhan, and C. Hu, "Noise modeling in BSIM6 compact model," in *Proc. Workshop Compact Model.*, Washington, DC, USA, Jun. 2014.
[25] (2014). *BSIM6.1.0 MOSFET Compact Model*. [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIM6_LR

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