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Analytical Modeling and Experimental Validation of Threshold Voltage in BSIM6 MOSFET Model

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ABSTRACT In this paper, an analytical model of threshold voltage for bulk MOSFET is developed. The model is derived from the physical charge-based core of BSIM6 MOSFET model, taking into account short channel effects, and is intended to be used in commercial SPICE simulators for operating point information. The model is validated with measurement data from IBM 90-nm technology node using various popular threshold voltage extraction techniques, and good agreement is obtained.

INDEX TERMS BSIM6, MOSFET, SPICE, threshold voltage.

I. INTRODUCTION

Threshold voltage is an important device parameter from modeling and circuit point of view, considering the fact that low power technologies are targeting the sub-threshold design. It is generally regarded as the signature of the technology and governs transition from weak inversion to strong inversion. Earlier generation MOSFET models, like BSIM3, BSIM4 etc, were based on the concept of threshold voltage. Although the state of the art modeling approaches (surface potential/charge based modeling) [1]–[4] do not endorse threshold voltage based methodologies, the fundamental physics essentially remains the same and still threshold voltage characterizes the technology. Classically, the threshold voltage is defined as the gate voltage at which the surface potential is $2\phi_f$, where ϕ_f is the bulk fermi potential [5]. However, one cannot measure the surface potential to calculate threshold voltage, but it has to be extracted. There are several methods proposed in literature to extract threshold voltage [6]–[10].

In this paper, we have develop an analytical model of threshold voltage for BSIM6 bulk MOSFET model, which can be used for operating point information in SPICE engines. Being a charge based model, BSIM6 does not use threshold voltage formulation. However, it is necessary to know threshold voltage of the transistor because circuit design techniques require it to bias the circuit in appropriate region, e.g., analog designer use it to bias the transistor in saturation region and digital designer needs it to determine on current. The model is validated with threshold voltage extracted from different exaction methods outlined in Section II. Rest of the paper is organized as follows. Section III presents the derivation of the proposed threshold voltage model. The results are reported in Section IV and the conclusion is drawn in Section V.

II. THRESHOLD VOLTAGE EXTRACTION METHODS

A. EXTRAPOLATION IN LINEAR REGION (ELR) [6]

This is the popular and widely used method of MOSFET characterization. In this method, I_D-V_G curve is linearly extrapolated from the point of maximum g_m (transconductance), and threshold voltage is given by its V_G intercept. For the saturation region, threshold voltage is extracted from the V_G intercept of linearly extrapolated $\sqrt{I_D}$-V_G curve, and the method is called as extrapolation in saturation region (ESR).

B. G_M/I_D [7]

This method defines threshold voltage as the gate voltage at which drift and diffusion components of the drain current are equal. Threshold voltage is extracted from $\frac{g_m}{I_D}$ vs V_G characteristics as a gate voltage corresponding to $\frac{g_m}{I_D} = 0.5\frac{g_m}{I_D}|_{max}$.

C. SECOND DERIVATIVE (SD) [8]

Also known as Transconductance Change method, it defines threshold voltage as the gate voltage corresponding to maximum slope of g_m-V_G characteristics. Threshold voltage in the saturation region is obtained from maximum slope of $\frac{d^2\sqrt{I_D}}{dV_g^2}$.

D. SECOND DERIVATIVE LOGARITHMIC (SDL) [9]

First derivative of the logarithm of drain current remains constant in weak inversion, and decays gradually to zero in strong inversion leading to minima of the second derivative in the vicinity of the transition region. In this method, threshold voltage is defined as the gate voltage where this double derivative is minimum.

E. CONSTANT CURRENT (CC) [10]

Owing to its simplicity, it is one of the most popular methods of threshold voltage extraction. Gate voltage corresponding to an arbitrary drain current given by $I_{CC} = \frac{W}{L}.I_0$ is defined as the threshold voltage. Here L, W are the effective channel length and width, respectively and I_0 is a constant current level chosen arbitrarily.

III. THRESHOLD VOLTAGE MODEL

A. LONG CHANNEL THRESHOLD VOLTAGE

The drain current under the standard drift-diffusion formalism can be represented as [11],

$$I_{ds} = I_{drift} + I_{diff} = -W.\mu\left(Q_i \cdot \frac{d\psi_s}{dx} + \cdot V_t\frac{dQ_i}{dx}\right) \quad (1)$$

where W, μ, Q_i, ψ_s and V_t represents channel width, mobility, inversion charge density, surface potential and thermal voltage respectively. Defining threshold voltage as the gate voltage at which $I_{drift} = I_{diff}$, using charge linearization [2], [4] and normalizing the inversion charge density to $-2n_qC_{ox}V_t$ leads to $q_i = \frac{1}{2}$, where q_i represents the normalized inversion charge density. Since inversion charge density varies along the channel from source to drain, depending on channel potential, source is chosen as reference and threshold voltage is defined as the gate voltage at which normalized inversion charge density at the source is given by

$$q_s = \frac{1}{2} \quad (2)$$

In BSIM6 model, pinch-off potential is first calculated from gate voltage, followed by inversion charge densities at source and drain ends [12]. Here, since q_i at threshold is known,

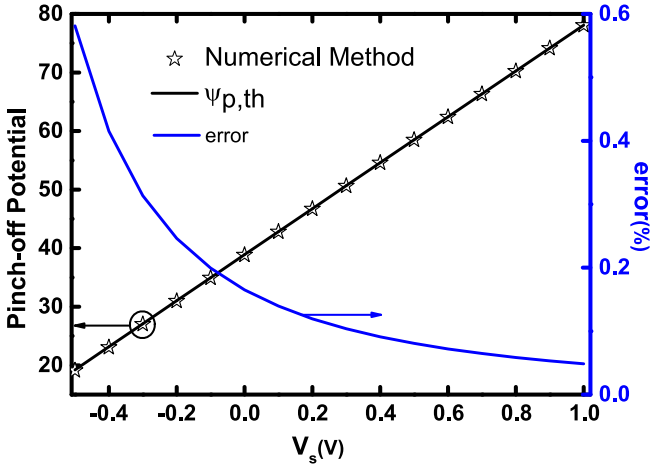

FIGURE 1. Comparison of $\psi_{p,th}$ (pinchoff potential at $q_s = 0.5$) with numerical solution. The source voltage is swept from −0.5 to 1 V. The error resulting from approximation in (5) is less than 1%, leading to compact, yet accurate expression of pinchoff potential at threshold condition.

the steps of BSIM6 core model are followed in reverse order. First, pinch-off potential corresponding to $q_s = \frac{1}{2}$ (represented as $\psi_{p,th}$) is calculated using the general relationship among q_i, pinch off potential (ψ_p) and channel potential (v_{ch}) [2]

$$\ln\left[\frac{2q_i.n_q}{\gamma_0}\left(q_i\frac{2n_q}{\gamma_0} + 2\sqrt{\psi_p - 2q_i}\right)\right] + 2q_i = \psi_p - 2\phi_f - v_{ch} \quad (3)$$

where the terms have their usual meanings. From (2) and (3),

$$\psi_{p,th} = 1 + \ln\left[\frac{n_q}{\gamma_0}l\left(\frac{n_q}{\gamma_0} + 2\sqrt{\psi_{p,th} - 1}\right)\right] + 2\phi_f + v_s \quad (4)$$

Note that above equation is implicit for $\psi_{p,th}$. To obtain it in explicit form, we make a simplifying assumption and replace $\psi_{p,th} - 1$ in RHS of (4) with $\psi_{p,th} - 1 = 2\phi_f + v_s$. The reason behind this assumption can be understand as follows. Classically, at threshold, $\psi_S = 2\phi_f + V_s$ and $Q_i = 0$. Since pinch-off potential is nothing but surface potential at $Q_i = 0$, this assumption can be used to approximate pinch-off potential at threshold. The other bias dependent term n_q is also approximated by $n_q = 1 + \frac{\gamma}{2\sqrt{2\phi_f + v_s}}$, which gives

$$\psi_{p,th} = 1 + \ln\left[\frac{n_q}{\gamma_0}l\left(\frac{n_q}{\gamma_0} + 2\sqrt{2\phi_f + v_s}\right)\right] + 2\phi_f + v_s \quad (5)$$

Fig. 1 shows comparison of pinch-off potential at $q_s = \frac{1}{2}$ obtained numerically from (4) and $\psi_{p,th}$ (obtained from (5)). The source voltage is swept from 0.5V to -1V. The error in $\psi_{p,th}$ remains less than 1% for the given body bias range which is fairly good in terms of accuracy. After $\psi_{p,th}$ is obtained, next step is to calculate threshold voltage. The potential balance equation in conjunction with Poisson's equation and Gauss's law for the MOSFET is given as [11],

$$V_G = V_{FB} + \psi_S - \frac{Q_{in} + Q_{dep}}{C_{ox}} \quad (6)$$

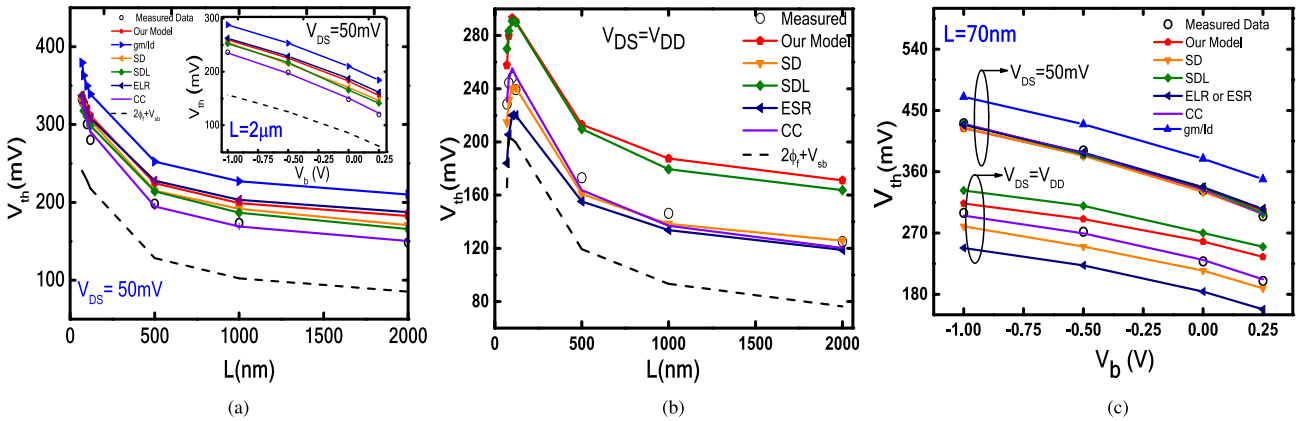

FIGURE 2. Threshold voltage model validation. (a) Threshold voltage versus channel length in linear region at $V_{ds} = 50$ mV and $V_b = 0$ V. Channel length is varied from 2 μm to 70 nm. The threshold voltage from the model is in close agreement with the extraction methods. It is also important to note that the model is able to capture the threshold voltage roll-up characteristics, typical to the halo implanted devices. Measured threshold voltage is extracted using CC method, for which $I_0 = 350$ nA is used. Inset figure shows the threshold voltage versus body bias in linear region at $V_{ds} = 50$ mV for $L = 2$ μm. (b) V_{th} versus L in saturation region. (c) V_{th} versus body bias in linear and saturation region. The model accurately models threshold voltage across length and drain and body biases.

where V_{FB} is the flat band voltage. At pinch-off, $\psi_S = \psi_P$, and $Q_{in} = 0$ [13], which gives

$$V_G = V_{FB} + \psi_P + \gamma\sqrt{\psi_P} \tag{7}$$

Thus we get final expression for long channel threshold voltage as

$$V_{th,long} = V_{FB} + \psi_{p,th}.V_t - \gamma\sqrt{\psi_{p,th}.V_t} \tag{8}$$

B. SHORT CHANNEL THRESHOLD VOLTAGE

Threshold voltage in short channel devices is affected by drain voltage, popularly known as drain induced barrier lowering (DIBL). Apart from DIBL, vertical non uniform doping (VNUD), Drain Induced Threshold Shift (DITS) also change threshold voltage. The compact models for threshold voltage shift were originally developed for BSIM3 and BSIM4 [14]–[16], and had gained popularity and wide acceptance in the device community. BSIM6 makes use of these models, with modification required for charge based formalism [13]. The effective threshold voltage for short channel devices is obtained as follows-

$$V_{th} = V_{th,long} - \Delta V_{th,DIBL} - \Delta V_{th,VNUD} - \Delta V_{th,DITS} \tag{9}$$

IV. SIMULATION RESULTS

The threshold voltage model is validated with IBM 90nm CMOS technology measurements for channel length varying from $2\mu m$ to $70nm$. We first extract DC modelcard for the set of devices under test, thereby fixing the parameter values in (9). Drain voltage for linear region operation is $50mV$ and for saturation region is V_{DD}, which is greater than 1V. To validate the model capability to capture threshold voltage across lengths, Fig. 2(a) shows the threshold voltage vs channel length, where channel length is varied from $2\mu m$ to $70nm$ at $V_{ds} = 50mV$ and $V_b = 0V$. Inset figure in Fig. 2(a) shows the threshold voltage vs body bias in linear region ($V_{ds} = 50mV$) for the long channel device ($L = 2\mu m$). The model is able to reproduce experimentally observed threshold voltage roll-up in Fig. 2(a), and is in agreement with the threshold voltage extracted from different extraction methods, especially with the popularly used constant current method.

Fig. 2(b) shows threshold voltage extracted in saturation region vs channel length at $V_{ds} = V_{DD}$ and $V_b = 0V$. Fig. 2(c) shows threshold voltage vs body bias for the short channel device ($L = 70nm$) biased in linear and saturation regions. The model accurately captures the drain and body bias effect on threshold voltage for short channel transistors. Fig. 2 also compares threshold voltage extracted from classical method ($Q_i = 0$) obtained using $\psi_s = 2\phi_f + v_s$. As observed in the Fig. 2, threshold voltage thus obtained is typically 50mV-100mV (2-4V_t at room temperature) below the threshold voltage extracted from other techniques. The proposed model, which is based on physical charge based core of BSIM6, allows to model threshold voltage in analytical form and its results are in close agreement with the extracted threshold voltage from different methods.

V. CONCLUSION

A new formulation of threshold voltage in BSIM6 model is presented. The model accounts for real device effects and utilizes charge based core of BSIM6 compact model. The model captures threshold voltage across lengths, drain and body biases, and shows excellent matching with the experimental data.

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